TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOSⅢ)

SSM6J23FE

High Current Switching Applications DC-DC Converter

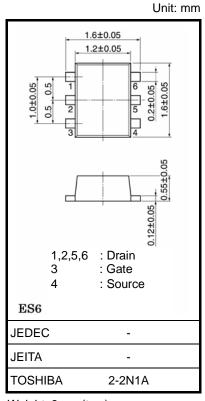
• Suitable for high-density mounting due to compact package

• Low on-resistance: $R_{on} = 160 \text{ m}\Omega \text{ (max) (@V_{GS} = -4.0 V)}$

 $R_{on} = 210 \text{ m}\Omega \text{ (max) (@VGS} = -2.5 \text{ V)}$

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V _{DS}	-12	V	
Gate-Source voltage		V _{GSS}	±8	V	
Drain current	DC	I _D	-1.2	А	
	Pulse	I _{DP}	-4.8		
Drain power dissipation		P _D (Note 1)	500	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55~150	°C	



Weight: 3 mg (typ.)

Note: Using continuously under heavy loads (e.g. the application of

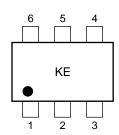
high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

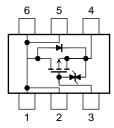
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board. (25.4 mm \times 25.4 mm \times 1.6 t, Cu Pad: 645 mm²)

Marking

Equivalent Circuit





Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic discharge. Operators should wear anti-static clothing and use containers and other objects that are made of anti-static materials.

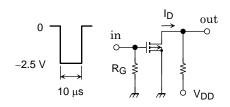
Electrical Characteristics (Ta = 25°C)

Chara	cteristics	Symbol	Test Condition	Min	Тур.	Max	Unit	
Gate leakage curr	ent	I _{GSS}	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0$	-	-	±1	μА	
Drain-Source breakdown voltage		V (BR) DSS	$I_D = -1 \text{ mA}, V_{GS} = 0$	-12	-	-	V	
		V (BR) DSX	$I_D = -1 \text{ mA}, V_{GS} = +8 \text{ V}$	-4	-	-	V	
Drain cut-off curre	ent	I _{DSS}	V _{DS} = -12 V, V _{GS} = 0	-	-	-1	μА	
Gate threshold voltage		V _{th}	V _{DS} = -3 V, I _D =-0.1 mA	-0.5	-	-1.1	V	
Forward transfer admittance		Y _{fs}	$V_{DS} = -3 \text{ V}, I_D = -0.6A$ (Note2)	1.75	3.5	-	S	
Drain-Source on-resistance		R _{DS (ON)}	$I_D = -0.6 \text{ A}, V_{GS} = -4 \text{ V}$ (Note2)) –	110	160	- mΩ	
			$I_D = -0.6 \text{ A}, V_{GS} = -2.5 \text{ V}$ (Note2)	_	145	210		
Input capacitance		C _{iss}	V _{DS} = -10 V, V _{GS} = 0, f = 1 MHz		420	-	pF	
Reverse transfer capacitance		C _{rss}	V _{DS} = -10 V, V _{GS} = 0, f = 1 MHz	_	75	-	pF	
Output capacitance		Coss	V _{DS} = -10 V, V _{GS} = 0, f = 1 MHz	_	93	-	pF	
Switching time	Turn-on time	t _{on}	$V_{DD} = -10 \text{ V}, I_D = -0.6 \text{A}$	-	23	-		
	Turn-off time	t _{off}	$V_{GS} = 0 \sim -2.5 \text{ V}, R_G = 4.7 \Omega$	=	30	_	ns	

Note2: Pulse test

Switching Time Test Circuit

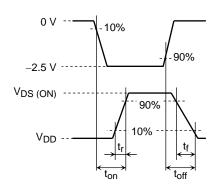




$$\begin{split} &V_{DD} = \text{-}10 \text{ V} \\ &R_G = 4.7 \text{ }\Omega \\ &\text{D.U.} \le 1\% \\ &V_{IN}\text{: }t_r, \, t_f < 5 \text{ ns} \\ &\text{Common Source} \\ &\text{Ta} = 25^{\circ}\text{C} \end{split}$$

(b) V_{IN}

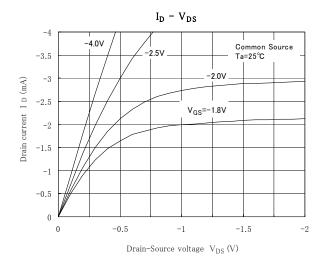
(c) V_{OUT}

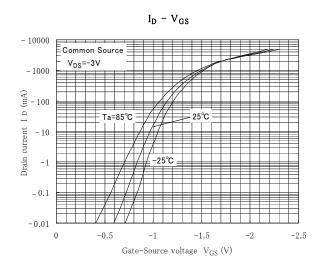


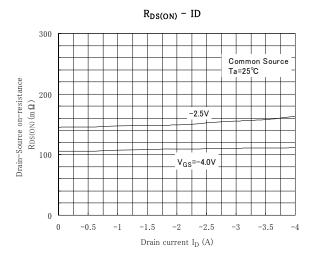
Precaution

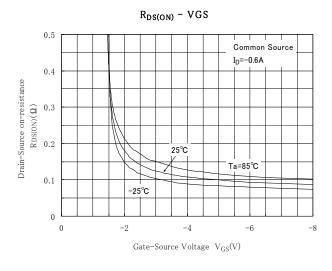
 V_{th} can be expressed as the voltage between gate and source when the low operating current value is $I_D = 100~\mu A$ for this product. For normal switching operation, V_{GS} (on) requires a higher voltage than V_{th} and V_{GS} (off) requires a lower voltage than V_{th} . (The relationship can be established as follows: V_{GS} (off) $< V_{th} < V_{GS}$ (on))

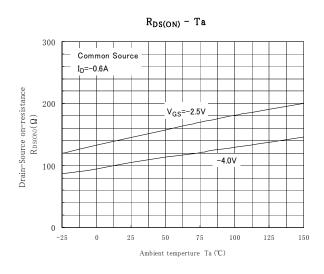
Please take this into consideration when using the device.

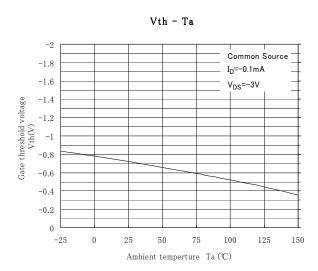


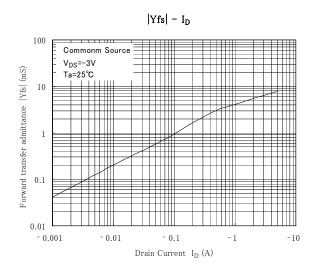


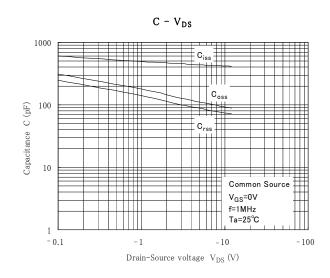


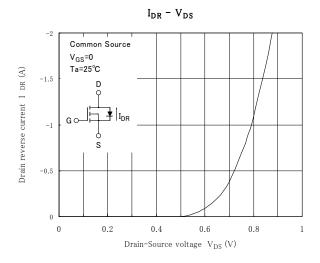


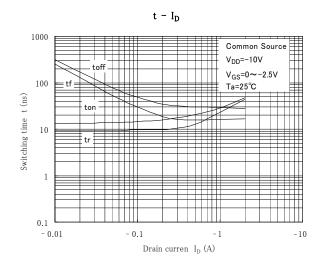


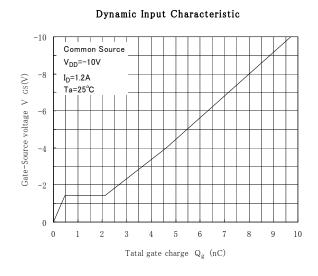


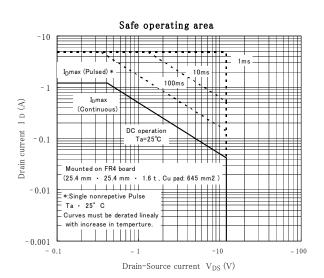


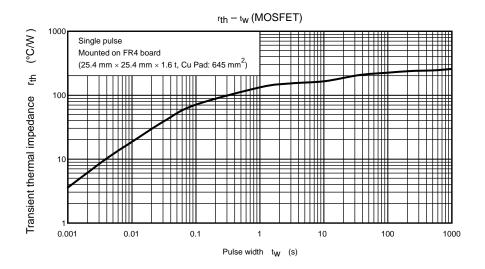


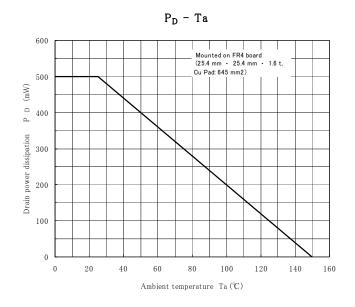












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