

## GENERAL DESCRIPTION

The ME2301A is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

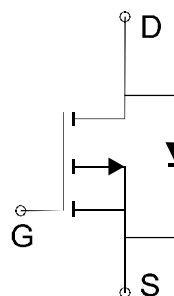
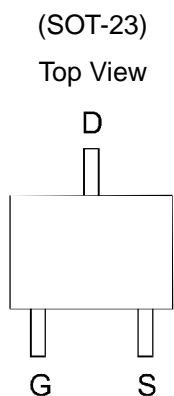
## FEATURES

- -20V/-2.8A,  $R_{DS(ON)}=75m\Omega@V_{GS}=-4.5V$
- -20V/-2.4A,  $R_{DS(ON)}=95m\Omega@V_{GS}=-2.5V$
- -20V/-1.7.0A,  $R_{DS(ON)}=130m\Omega@V_{GS}=-1.8V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

## APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

## PIN CONFIGURATION



## Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DSS}$	-20	V
Gate-Source Voltage	$V_{GSS}$	±12	V
Continuous Drain Current (tJ=150°C)	$I_D$	$T_A=25^\circ C$	-2.8
		$T_A=70^\circ C$	-2.0
Pulsed Drain Current	$I_{DM}$	-10	A
Maximum Power Dissipation	$P_D$	$T_A=25^\circ C$	1.4
		$T_A=70^\circ C$	1
Operating Junction Temperature	$T_J$	-55 to 150	°C
Storage Temperature Range	$T_{stg}$	-55 to 150	°C
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	$T \leq 10$ sec	75
		Steady State	100
Thermal Resistance-Junction to Case	$R_{\theta JC}$	65	°C/W

\* The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper

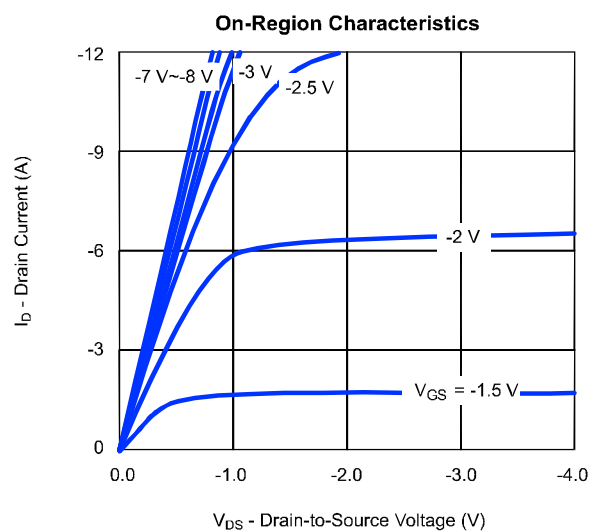
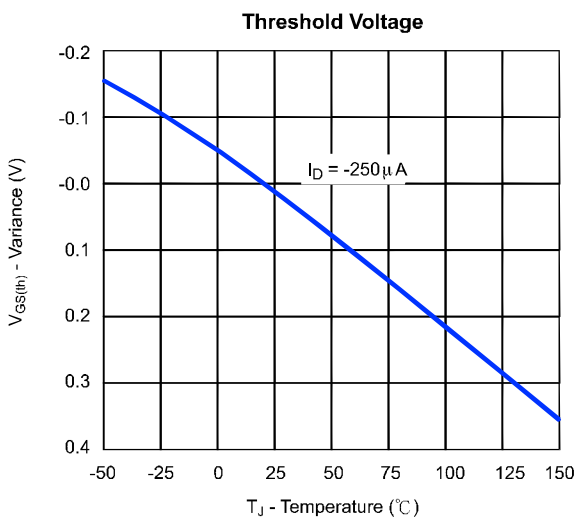
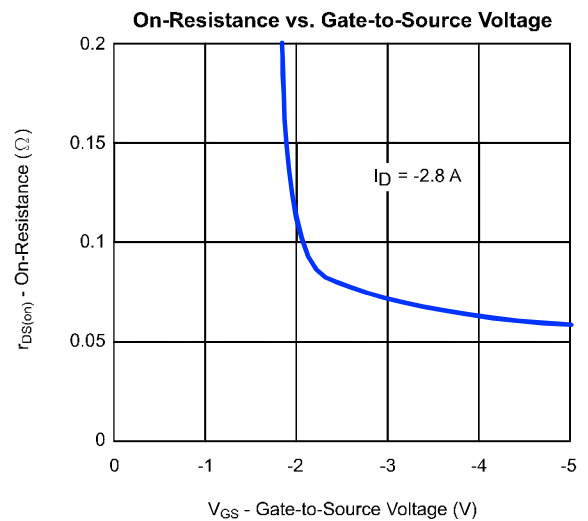
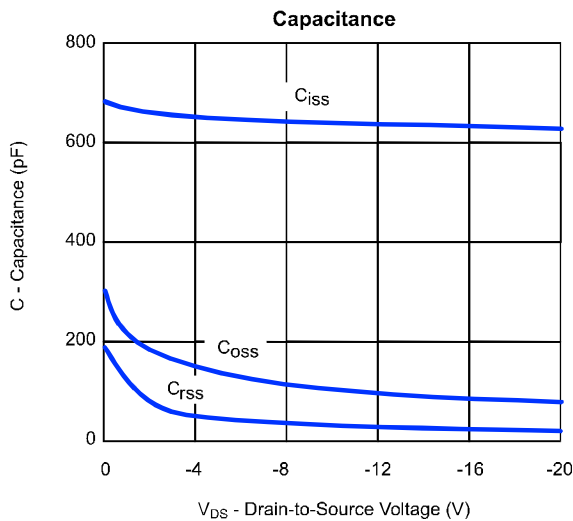
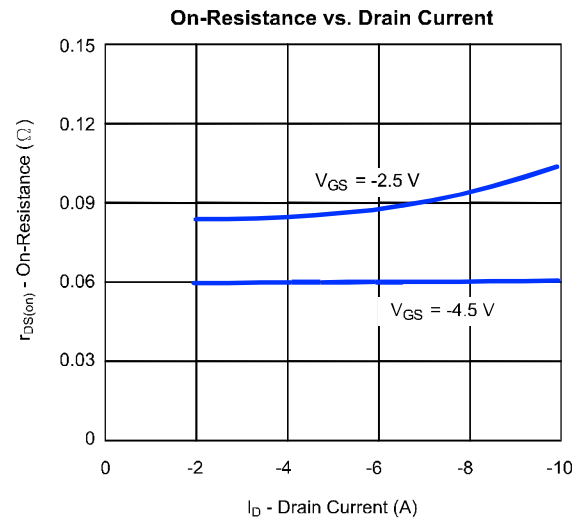
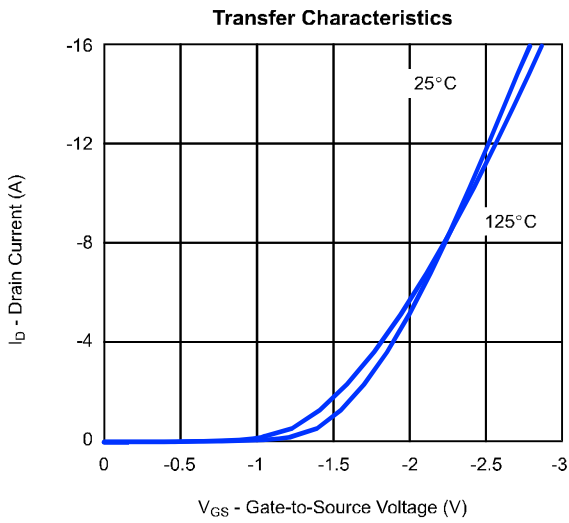
## P-Channel Enhancement Mode Mosfet

Electrical Characteristics (TA=25°C Unless Otherwise Specified)

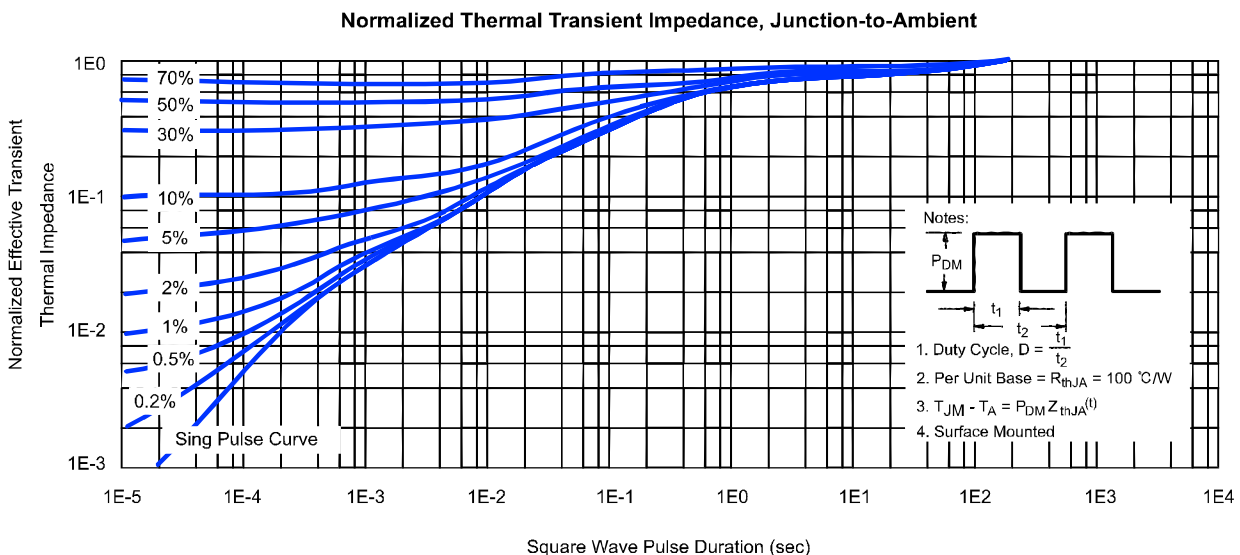
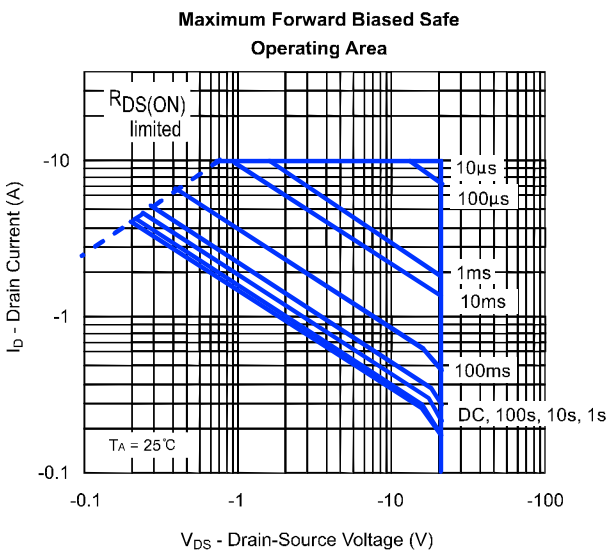
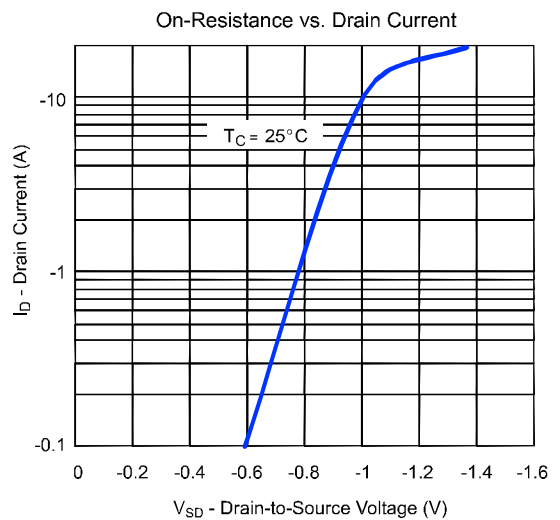
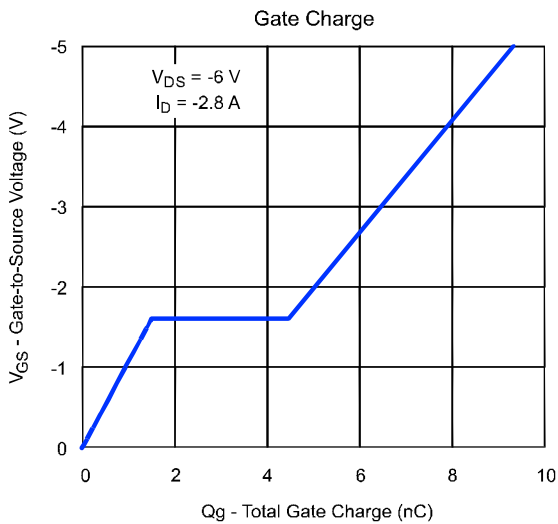
Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250 μA	-20			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250 μA	-0.4	-0.6	-0.9	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±12V			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V			-1	μA
I <sub>D(ON)</sub>	On-State Drain Current <sup>a</sup>	V <sub>DS</sub> =-5V, V <sub>GS</sub> = -10V	-6			A
R <sub>DS(ON)</sub>	Drain-Source On-Resistance <sup>a</sup>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> = -2.8A		55	75	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> = -2.4A		70	95	
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> = -1.7A		100	130	
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.7	-1	V
<b>DYNAMIC</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-6V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A		9	11	nC
Q <sub>gs</sub>	Gate-Source Charge			2.3		
Q <sub>gd</sub>	Gate-Drain Charge			2		
R <sub>g</sub>	Gate resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz		6		Ω
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz		650	680	pF
C <sub>oss</sub>	Output Capacitance			120		
C <sub>rss</sub>	Reverse Transfer Capacitance			38		
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DS</sub> =-6V, R <sub>L</sub> =3.6Ω R <sub>GEN</sub> =6Ω, V <sub>GS</sub> =-4.5V		38	45	ns
t <sub>r</sub>	Turn-On Rise Time			25	30	
t <sub>d(off)</sub>	Turn-Off Delay Time			43	50	
t <sub>f</sub>	Turn-Off Fall time			5	7	

Notes: a. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%

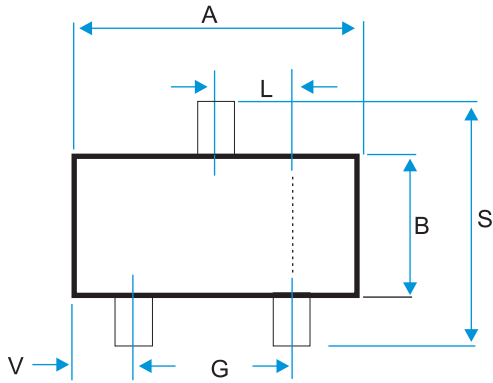
Typical Characteristics (T<sub>J</sub> = 25°C Noted)



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### SOT-23 Package Outline



DIM	MILLIMETERS	
	MIN	MAX
A	2.80	3.1
B	1.20	1.7
C	0.89	1.3
D	0.37	0.50
G	1.78	2.04
H	0.013	0.15
J	0.085	0.2
K	0.45	0.7
L	0.89	1.02
S	2.10	3
V	0.45	0.60

