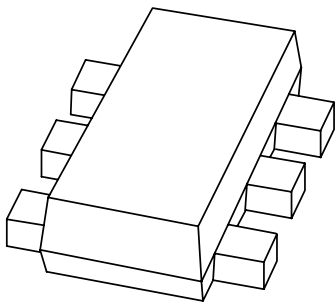


DATA SHEET



PEMD3

**NPN/PNP resistor-equipped
transistors; R1 = 10 k Ω , R2 = 10 k Ω**

Product specification
Supersedes data of 2001 Sep 13

2001 Nov 07

**NPN/PNP resistor-equipped transistors;
R1 = 10 kΩ, R2 = 10 kΩ**

PEMD3

FEATURES

- 300 mW total power dissipation
- Very small 1.6 mm x 1.2 mm ultra thin package
- Excellent coplanarity due to straight leads
- Replaces two SC-75/SC-89 packaged transistors on same PCB area
- Reduces required PCB area
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

DESCRIPTION

NPN/PNP resistor-equipped transistors in a SOT666 plastic package.

MARKING

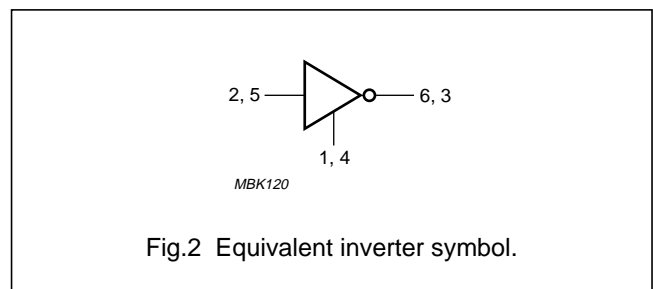
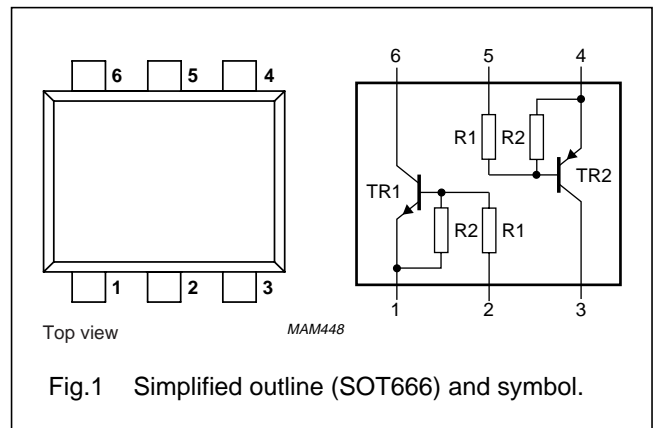
TYPE NUMBER	MARKING CODE
PEMD3	D3

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V _{CEO}	collector-emitter voltage	50	V
I _{CM}	peak collector current	100	mA
TR1	NPN	–	–
TR2	PNP	–	–
R1	bias resistor	10	kΩ
R2	bias resistor	10	kΩ

PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2



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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity					
V _{CBO}	collector-base voltage	open emitter	–	50	V
V _{CEO}	collector-emitter voltage	open base	–	50	V
V _{EBO}	emitter-base voltage	open collector	–	10	V
V _I	input voltage TR1	positive	–	+40	V
		negative	–	–10	V
	input voltage TR2	positive	–	+10	V
		negative	–	–40	V
I _O	output current (DC)		100	mA	
I _{CM}	peak collector current		100	mA	
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C
Per device					
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	300	mW

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	notes 1 and 2	416	K/W

Notes

1. Transistor mounted on an FR4 printed-circuit board.
2. The only recommended soldering method is reflow soldering.

NPN/PNP resistor-equipped transistors;
 $R_1 = 10 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$

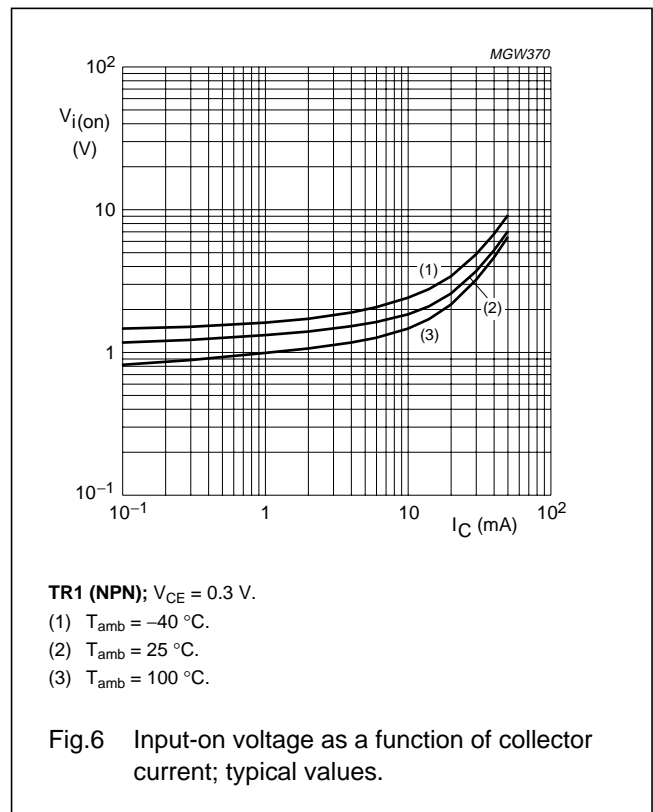
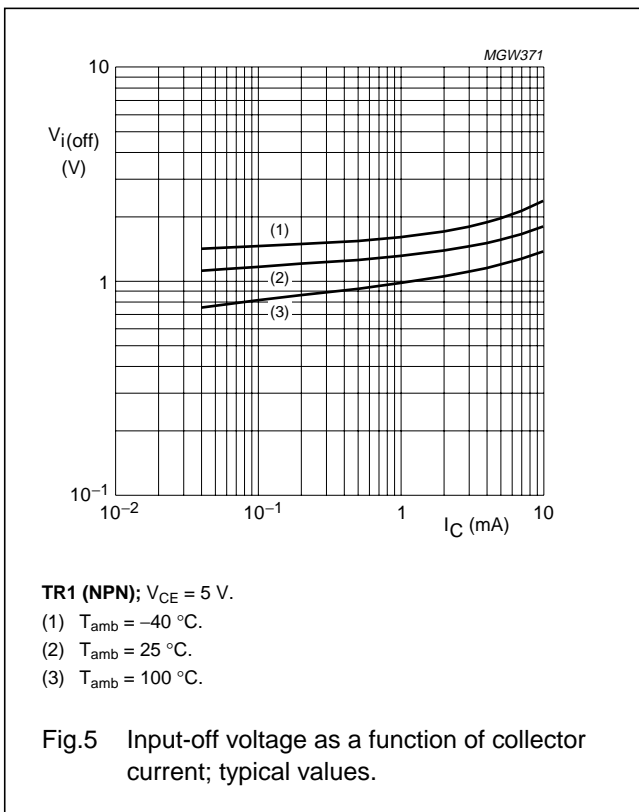
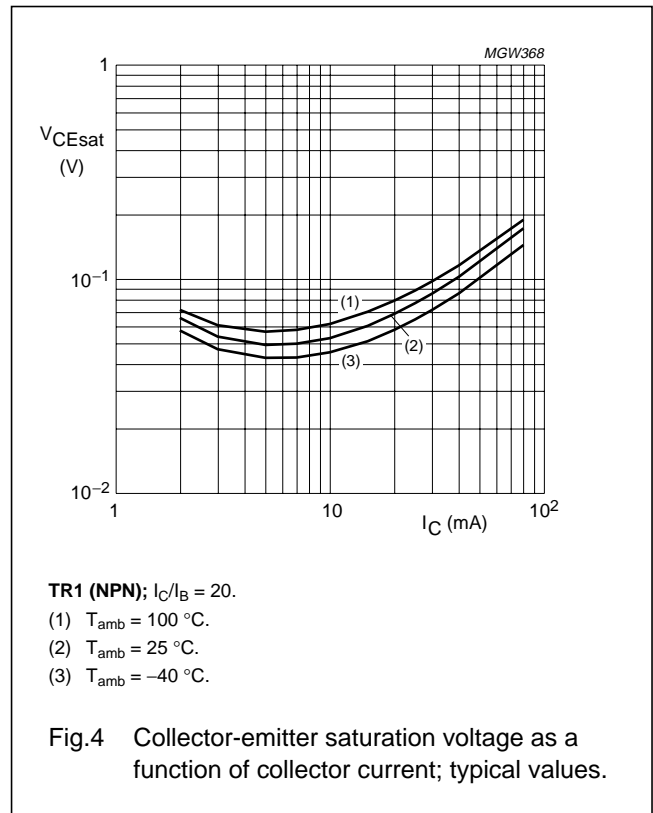
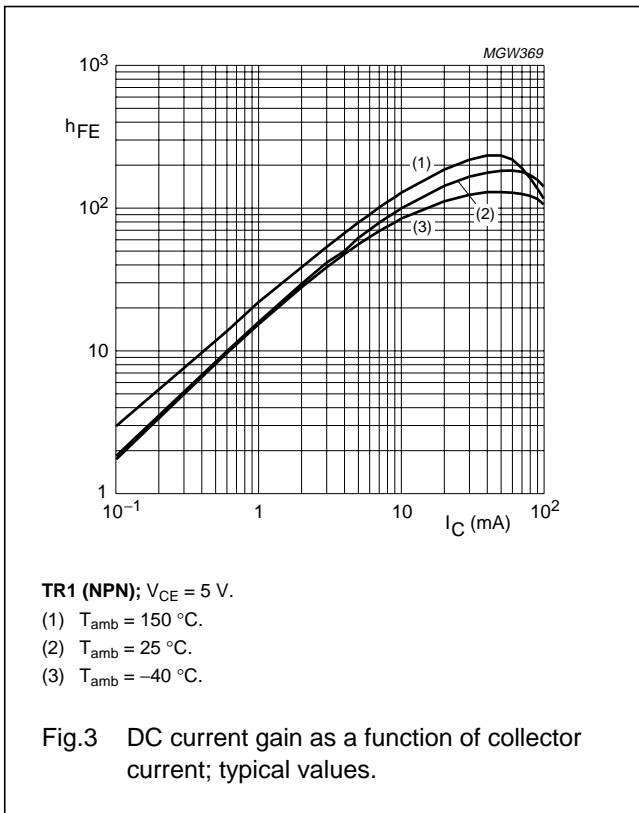
PEMD3

CHARACTERISTICS $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity						
I_{CBO}	collector-base cut-off current	$V_{\text{CB}} = 50 \text{ V}$; $I_{\text{E}} = 0$	–	–	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{\text{CE}} = 50 \text{ V}$; $I_{\text{B}} = 0$	–	–	1	μA
		$V_{\text{CE}} = 30 \text{ V}$; $I_{\text{B}} = 0$; $T_{\text{j}} = 150 \text{ }^\circ\text{C}$	–	–	50	μA
I_{EBO}	emitter-base cut-off current	$V_{\text{EB}} = 5 \text{ V}$; $I_{\text{C}} = 0$	–	–	400	μA
h_{FE}	DC current gain	$V_{\text{CE}} = 5 \text{ V}$; $I_{\text{C}} = 5 \text{ mA}$	30	–	–	
V_{CEsat}	saturation voltage	$I_{\text{C}} = 10 \text{ mA}$; $I_{\text{B}} = 0.5 \text{ mA}$	–	–	150	mV
$V_{\text{i(off)}}$	input off voltage	$V_{\text{CE}} = 5 \text{ V}$; $I_{\text{C}} = 100 \mu\text{A}$	–	1.1	0.8	V
$V_{\text{i(on)}}$	input on voltage	$V_{\text{CE}} = 0.3 \text{ V}$; $I_{\text{C}} = 10 \text{ mA}$				
	TR1 (NPN)		2.5	1.1	–	V
	TR2 (PNP)		2.5	1.8	–	V
R_1	input resistor		7	10	13	$\text{k}\Omega$
$\frac{R_2}{R_1}$	resistor ratio		0.8	1	1.2	
C_{c}	collector capacitance	$I_{\text{E}} = i_{\text{e}} = 0$; $V_{\text{CB}} = 10 \text{ V}$; $f = 1 \text{ MHz}$			2.5	pF
	TR1 (NPN)		–	–	3	pF
	TR2 (PNP)		–	–		

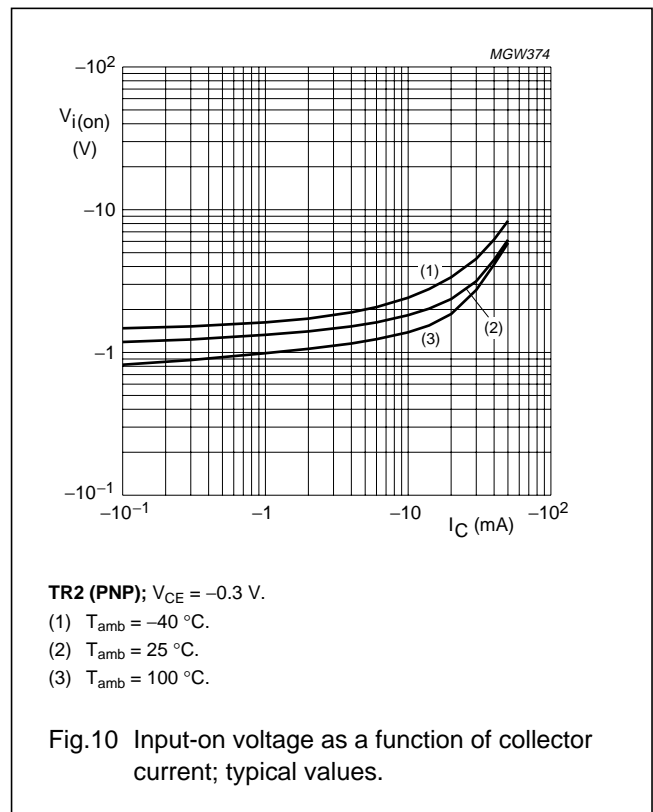
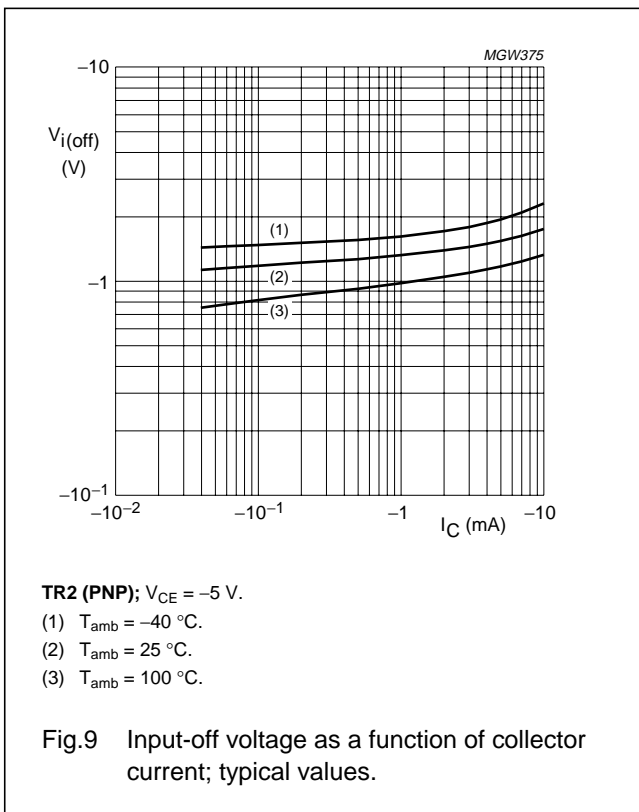
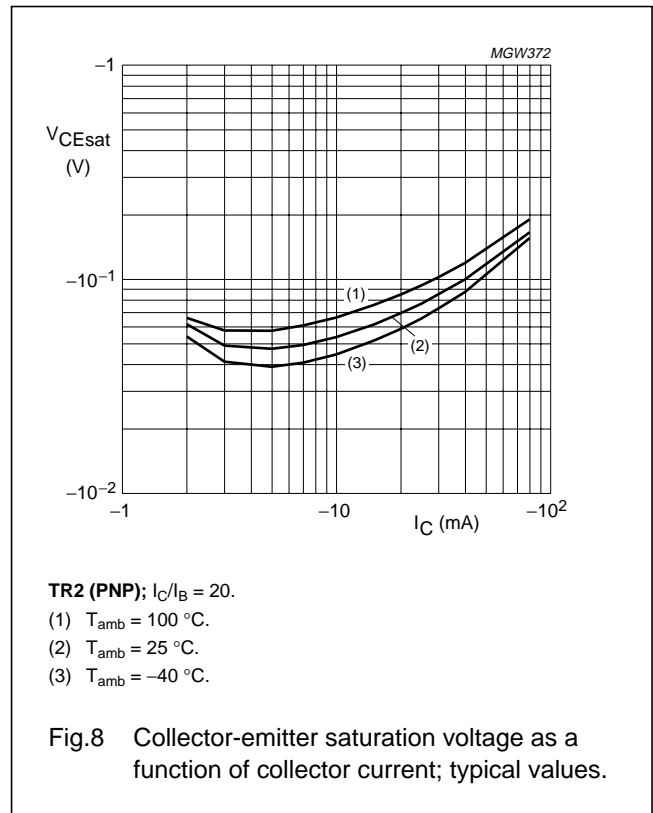
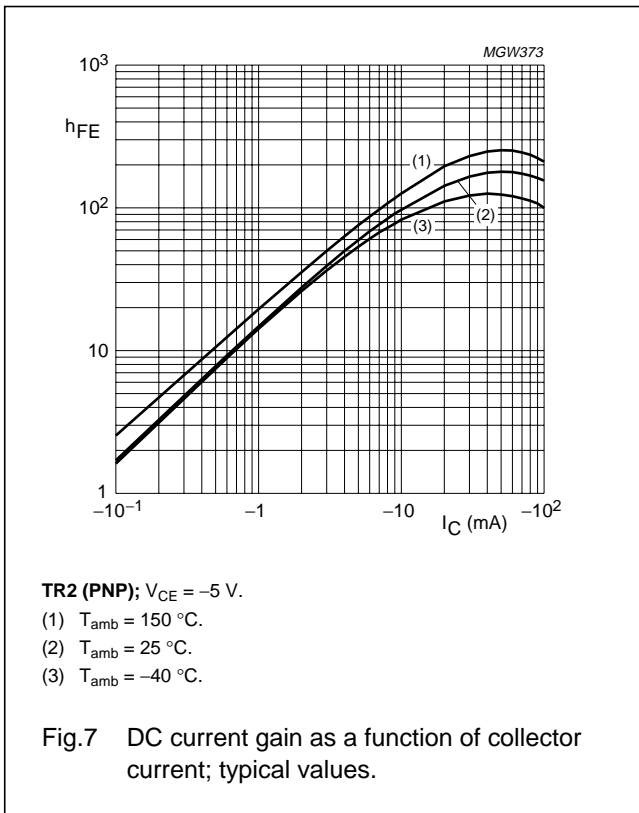
NPN/PNP resistor-equipped transistors;
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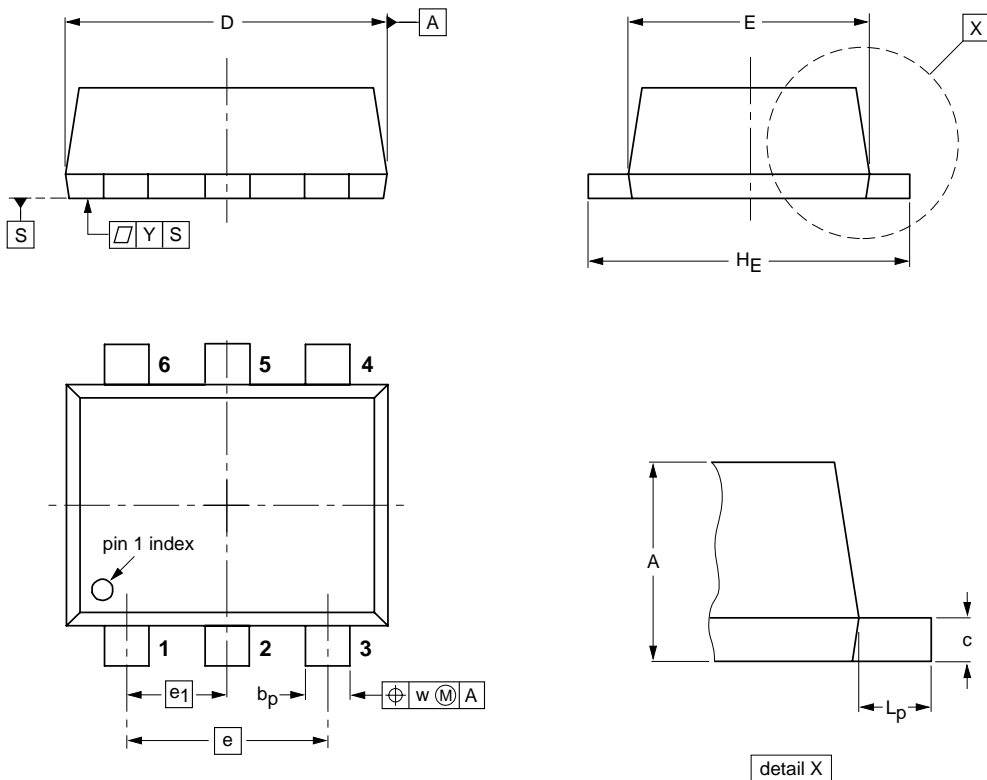
NPN/PNP resistor-equipped transistors;
R1 = 10 kΩ, R2 = 10 kΩ

PEMD3

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	b _p	c	D	E	e	e ₁	H _E	L _p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT666						01-01-04 01-08-27

NPN/PNP resistor-equipped transistors;
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PEMD3

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NOTES

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NOTES

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