National Semiconductor

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LP3987
Micropower micro SMD 150 mA Ultra Low-Dropout CMOS Voltage Regulators with sleep MODE

General Description

The LP3987 is a 150mA fixed output voltage regulator with very low dropout voltage designed specially to meet requirements of battery-powered applications. The additional sleep MODE feature will reduce current consumption during standby operation to prolong the usage of battery.

Dropout Voltage: 100mV maximum dropout with 150mA load.

Shutdown: Less than 1µA quiescent current.

Sleep Mode: Typically 14µA quiescent current during sleep MODE to reduce battery consumption.

Enhanced Stability: The LP3987 is stable with minimum 1µF±20% low ESR ceramic output capacitor as low as 5mΩ and high quality tantalum capacitors.

The LP3987 is available in thin and thick 5 Bump micro SMD package. Performance is specified for –40˚C to 125˚C.

This device is available with output voltage options of 2.6V, 2.8V, & 2.85V. For other voltage options, please contact National Semiconductor Corporation.

Features

- Miniature 5-I/O micro SMD package
- Stable with ceramic and high quality tantalum output capacitors
- Logic controlled enable
- Thermal Shutdown and short-circuit current limit

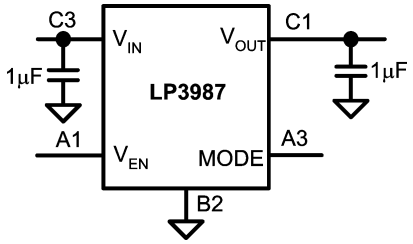
Key Specifications

- 2.7 to 6.0V input range
- Guaranteed 150 mA output current
- 1µA quiescent current on shutdown
- 100 mV maximum dropout with 150 mA load
- 50dB PSRR at 10KHz
- Sleep MODE features
- Over temperature & over current protection
- –40˚C to +125˚C junction temperature range for operation

Applications

- CDMA cellular handsets
- Wideband CDMA cellular handsets
- GSM cellular handsets
- Portable information appliances
- µP/DSP Power Supplies
- Digital Cameras
- SRAM Backup

Typical Application Circuit



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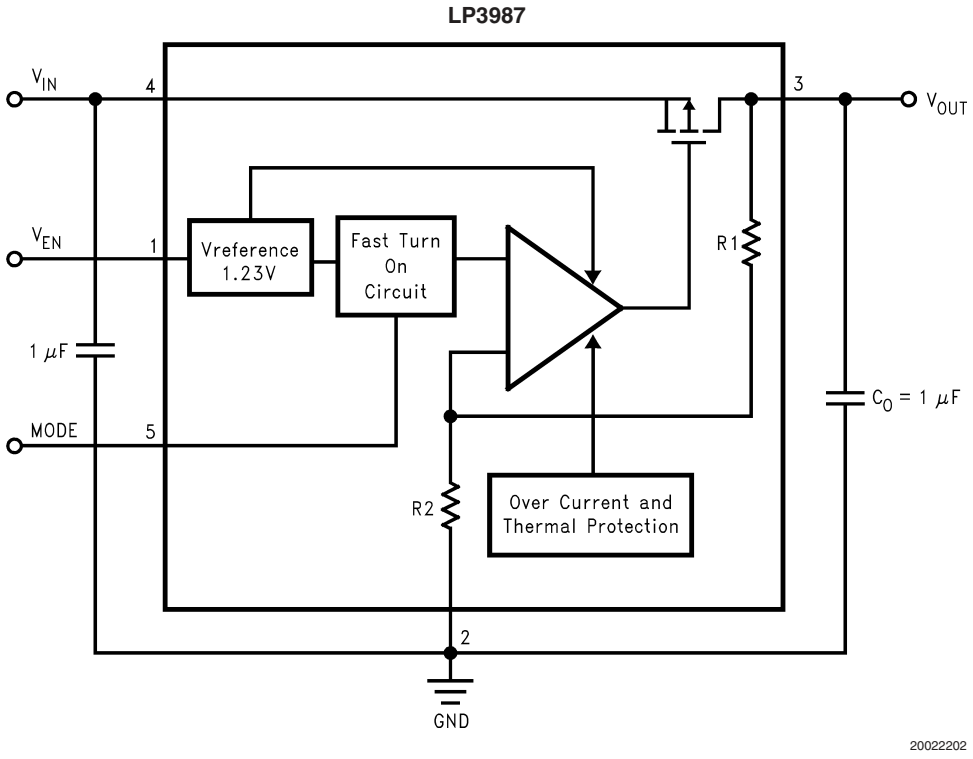
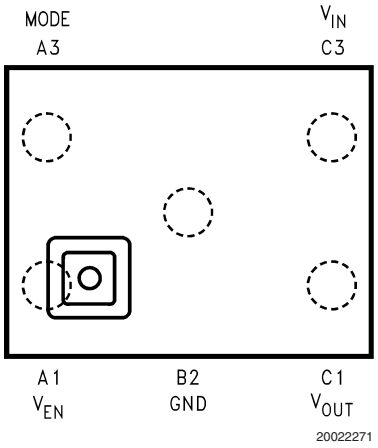
Block Diagram



Connection Diagram



Top View
5 I/O micro SMD Package
See NS Package Number BPA05/TLA05/BLA05

Pin Descriptions

Name	micro SMD*	Function
V_{EN}	A1	Enable Input Logic, Enable High
GND	B2	Common Ground
V_{OUT}	C1	Output voltage of the LDO
V_{IN}	C3	Input voltage of the LDO
MODE	A3	Power Mode Control, Active = 1, Sleep Mode = 0

* The pin numbering scheme for the micro SMD package was revised in April, 2002 to conform to JEDEC standard. Only the pin numbers were revised. No changes to the physical location of the inputs/outputs were made. For reference purposes, the obsolete numbering scheme had VEN as pin 1, GND as pin 2, VOUT as pin 3, VIN as pin 4, and MODE as pin 5.

Ordering Information

BP refers to a 0.170mm bump size with package height of 0.9mm

Output Voltage (V)	Grade	LP3987 Supplied as 250 Units, Tape and Reel	LP3987 Supplied as 3000 Units, Tape and Reel
2.85*	STD	LP3987IBP-2.85	LP3987IBPX-2.85

* Please contact National Semiconductor for availability

BL refers to a 0.300mm bump size with package height of 0.9mm

Output Voltage (V)	Grade	LP3987 Supplied as 250 Units, Tape and Reel	LP3987 Supplied as 3000 Units, Tape and Reel
2.85	STD	LP3987IBL-2.85	LP3987IBLX-2.85

* Please contact National Semiconductor for availability

TL refers to a 0.300mm bump size with package height of 0.6mm

Output Voltage (V)	Grade	LP3987 Supplied as 250 Units, Tape and Reel	LP3987 Supplied as 3000 Units, Tape and Reel
2.5	STD	LP3987ITL-2.5	LP3987ITLX-2.5
2.6	STD	LP3987ITL-2.6	LP3987ITLX-2.6
2.8	STD	LP3987ITL-2.8	LP3987ITLX-2.8
2.85	STD	LP3987ITL-2.85	LP3987ITLX-2.85
3.0*	STD	LP3987ITL-3.0	LP3987ITLX-3.0

* Please contact National Semiconductor for availability

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN}	−0.3 to 6.5V
V_{EN}, V_{MODE}	−0.3 to 6.5V
V_{OUT}	−0.3V to(V_{IN}+ 0.3V) ≤ 6.5
Storage Temperature	−65˚C to +150˚C
ESD (Note 4)	
Human Body Model	2KV
Machine Model	200V
Maximum Power Dissipation (Note 3)	
θ_{JA} (micro SMD small bump)	255˚C/W

Operating Ratings (Notes 1, 2)

V_{IN}	V_{OUT}+ 200mV to 6V
V_{EN}, V_{MODE}	0 to 6.0V
Junction Temperature	−40˚C to +125˚C
Maximum Power Dissipation (Note 3)	392mW at 25˚C

Electrical Characteristics

Unless otherwise specified: V_{EN} = 1.8V, MODE = 1.8V, V_{IN} = $V_{OUT(nom)}$ + 0.5V, C_{IN} = 1 µF, I_{OUT} = 1mA, C_{OUT} = 1 µF. Typical values and limits appearing in standard typeface are for T_J = 25˚C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40˚C to +125˚C. (Note 10) (Note 11)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
ΔV_{OUT}	Output Voltage Tolerance	I_{OUT} = 1mA, 25˚C		-2	2	% of $V_{OUT(nom)}$
		I_{OUT} = 1mA		**−3**	**3**	
	Line Regulation Error	V_{IN} = ($V_{OUT(nom)}$ + 0.5V) to 6.0V, I_{OUT} = 1 mA		**−0.1**	**0.1**	%/V
	Load Regulation Error	I_{OUT} = 1mA to 150 mA		0.0004	**0.002**	%/mA
	Dropout Voltage (Note 6)	I_{OUT} = 1mA	0.4		**2**	mV
		I_{OUT} = 150mA	60		**100**	
$\Delta V_{OUT(SLEEP)}$	Output Voltage difference at MODE = 0V	MODE = 0V, (Note 7)		**-150**	**+100**	mV
Transient Response	Line Transient Response (Note 5)	MODE = 1.8V, I_{LOAD} = 100mA, T_{RISE} = T_{FALL} = 10µS, V_{IN} = 600mV $_{P-P}$ AC Square wave, (Note 8)	21			mVpp
	Load Transient Response (Note 5)	MODE = 1.8V, C_{OUT} = 4.7µF, T_{RISE} = T_{FALL} = 100nS, V_{IN} = 3.1V, 3.6V, 4.2V, (Notes 9, 12)	100			mVpk
PSRR	Power Supply Rejection Ratio (Note 5)	V_{IN} = $V_{OUT(nom)}$ + 1V, MODE = 1.8V, f = <10 kHz, I_{OUT} = 1mA	50			dB
		V_{IN} = $V_{OUT(nom)}$ + 1V, MODE = 0V, f = <10 kHz, I_{OUT} = 1mA	10			
$I_{Q(ON)}$	Quiescent Current	MODE = 1.8V, I_{OUT} = 0mA, V_{IN} = 4.2V	85		**120**	µA
		MODE = 1.8V, I_{OUT} = 150mA, V_{IN} = 4.2V	160		**200**	
$I_{Q(OFF)}$	Quiescent Current	ENABLE = 0V, V_{IN} = 4.2V	1		**3**	µA
$I_{Q(SLEEP)}$	Current in Standby Mode	MODE = 0V, I_{OUT} = 50µA, V_{IN} = 4.2V	14		**21**	µA
I_{SC}	Short Circuit Current Limit (Note 5)	Output Grounded	600			mA

Electrical Characteristics (Continued)

Unless otherwise specified: V_{EN} = 1.8V, MODE = 1.8V, V_{IN} = $V_{OUT(nom)}$ + 0.5V, C_{IN} = 1 µF, I_{OUT} = 1mA, C_{OUT} = 1 µF. Typical values and limits appearing in standard typeface are for T_J = 25˚C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40˚C to +125˚C. (Note 10) (Note 11)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
$I_{SC(SLEEP)}$	Short Circuit Current in Sleep MODE	Output Grounded	28		**43**	mA
$I_{OUT(ON)}$	Maximum Output Current at MODE = 1.8V	MODE = 1.8V		**150**		mA
$I_{OUT(SLEEP)}$	Maximum Output Current at MODE = 0V	MODE = 0V		**3**		mA
e_n	Output Noise Voltage, (Note 5)	BW = 10 Hz to 100 kHz, C_{OUT} = 1µF	70			µVrms
$T_{SHUTDOWN}$	Shutdown Temperature (Note 5)	Sleep MODE = 1.8V	155			˚C
Logic Control Characteristics						
I_{EN}	Maximum Input Current at EN	V_{EN} = 0 and V_{IN}= 6.0V	0.015			µA
V_{IL}	Logic Low Input Threshold	V_{IN} = 3.05 to 6V		**0.5**		V
V_{IH}	Logic High Input Threshold	V_{IN} = 3.05 to 6V			**1.2**	V
V_{MODE_L}	Logic Low Input Threshold	V_{IN} = 3.05 to 6V		**0.5**		V
V_{MODE_H}	Logic High Input Threshold	V_{IN} = 3.05 to 6V			**1.2**	V
I_{MODE}	Maximum Input Current at V_{MODE}	V_{MODE} = 0 and V_{IN} = 6.0V	0.015			µA
Timing Characteristics						
T_{ON}	Turn on Time (On Mode), (Notes 5, 13)	MODE = 1.8V, C_{OUT} = 4.7µF	170		**250**	µs
T_{SLEEP}	Turn on Time (Sleep Mode), (Note 5), (Note 14)	MODE = 0V, C_{OUT} = 4.7µF	0.5		**5**	ms
T_{MODE}	Sleep to On Mode Settle Time, (Note 5), (Note 15)	C_{OUT} = 4.7µF, Enable = 1.8V	200		**300**	µs

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula:

$$P_D = (T_J - T_A)/\theta_{JA},$$

Where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. For instant, if V_{IN} in target application is 4.2V and worse case current consumption is 90mA. Therefore $P_{MAX\_DISSIPATION}$ = (4.2-2.7)*0.09 =135mW. With $P_{MAX\_DISSIPATION}$ is 135mW, T_{Jmax} is 125˚C and worse case ambient temperature (TA) in target application is 85˚C, θ_{JA} = (125-85)/0.135 = 296˚C/W.

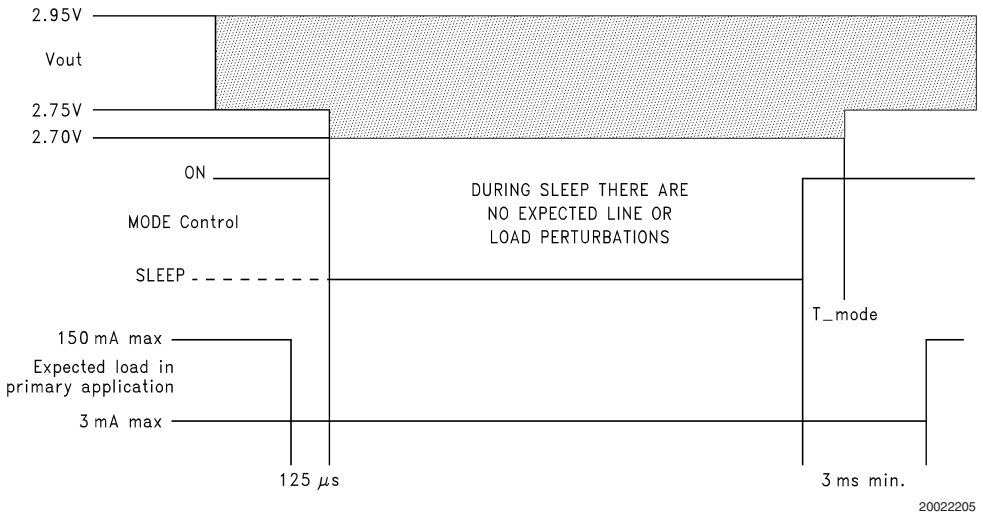
Note 4: The human body model is 100pF discharged through 1.5kΩ.

Note 5: This electrical specification is guaranteed by design.

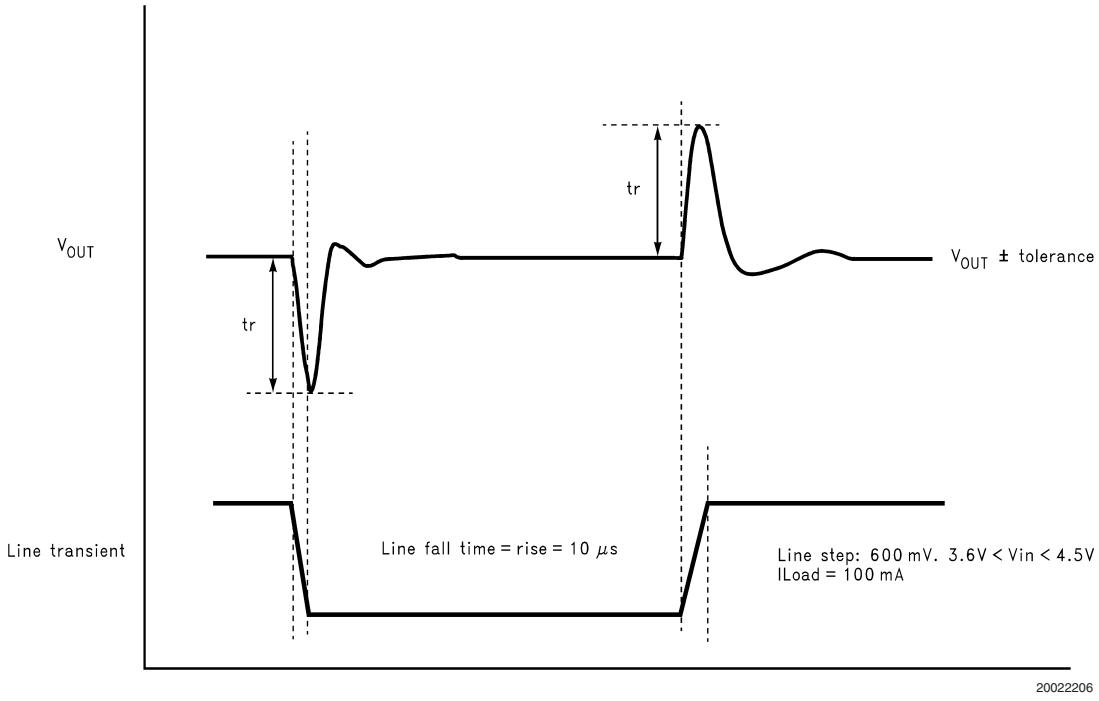
Electrical Characteristics (Continued)

Note 6: Dropout voltage is defined as the input to output voltage differential at which the output voltage falls to 100mV below the nominal output voltage. V_{IN} less than minimum operating voltage may be used for test purposes.

Note 7: On/Sleep Mode voltage tolerance and current capability requirement.

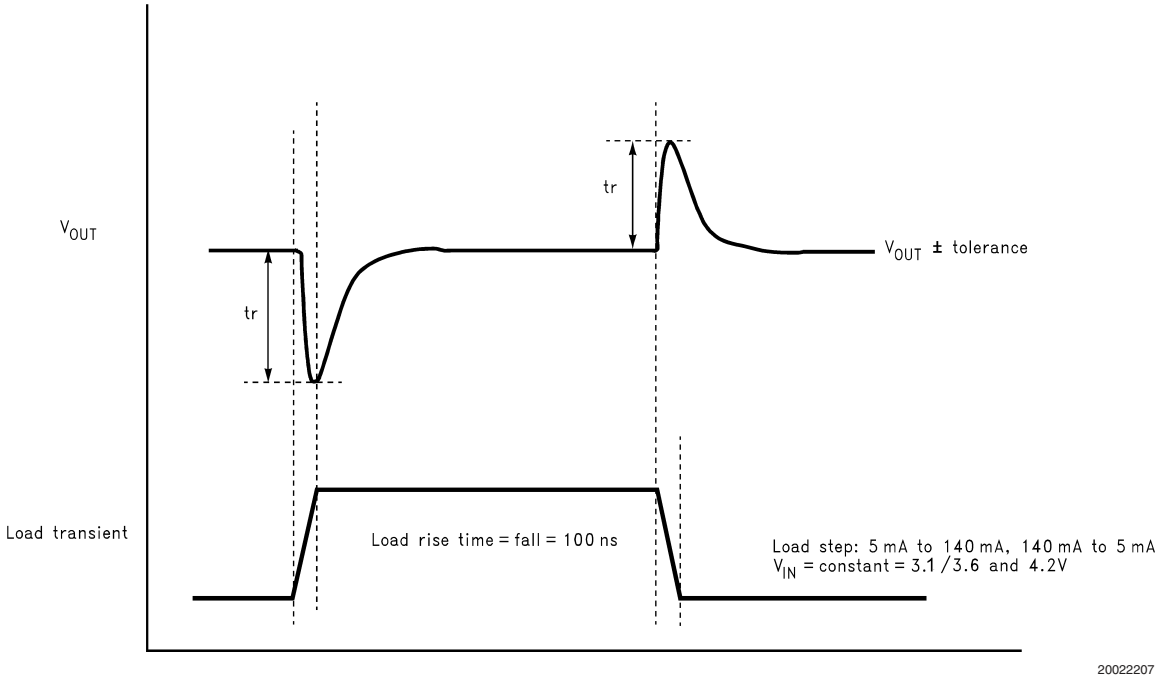


Note 8: Line Transient response requirement:



Electrical Characteristics (Continued)

Note 9: Load Transient response requirement:



Note 10: All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with T_J = 25˚C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 11: The nominal output voltage, which is labeled $V_{OUT(nom)}$, is the output voltage measured with the input 0.5V above $V_{OUT(nom)}$ and a 1mA load.

Note 12: During transient recovery, output voltage should not be oscillating.

Note 13: T_{ON} is measured from rising edge of Enable with MODE = 1.8V to when V_{OUT} reaches 95% of final value.

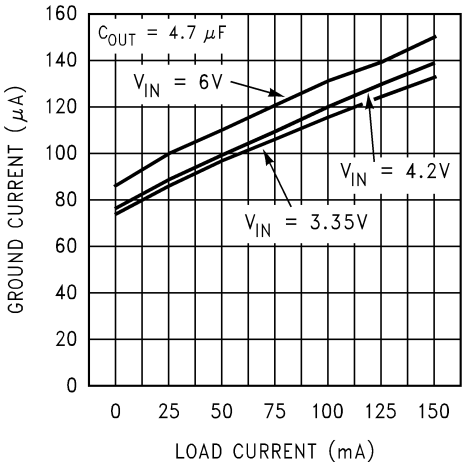
Note 14: T_{SLEEP} is measured from rising edge of Enable with MODE = 0V to when V_{OUT} reaches 95% of final value.

Note 15: T_{MODE} is measured from rising edge of MODE with ENABLE = 1.8V to time before full current capability.

Typical Performance Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 1\ \mu F$ Ceramic, $V_{IN} = V_{OUT(nom)} + 0.5V$, $T_A = 25^{\circ}C$, Enable pin is tied to V_{IN}, MODE = 1.8V.

Ground Current @ $T_A = 25^{\circ}C$



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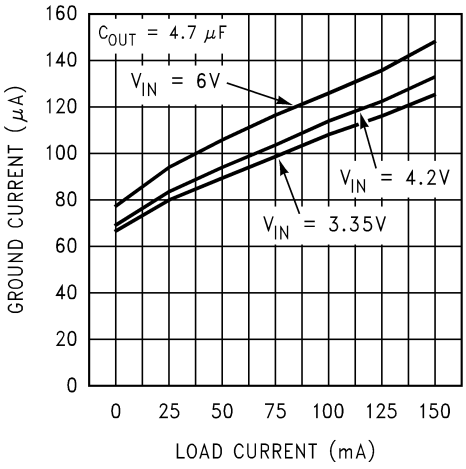
Ground Current @ $T_A = 40^{\circ}C$



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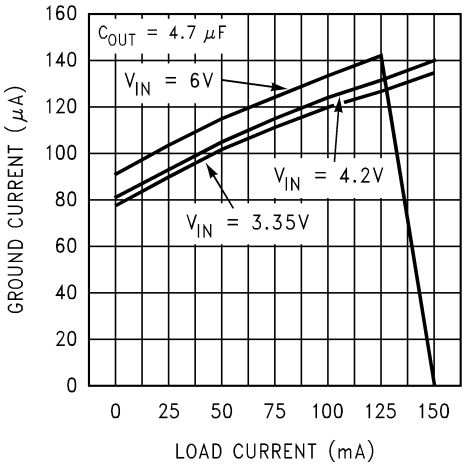
Ground Current @ $T_A = 85^{\circ}C$



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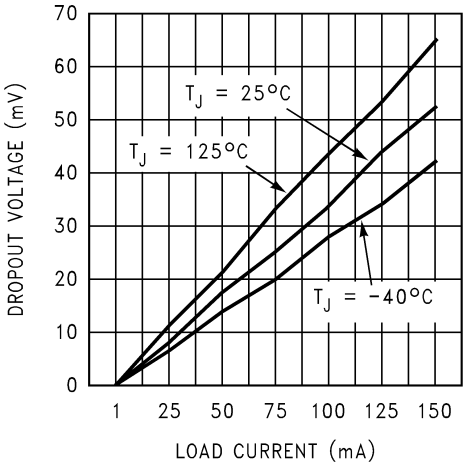
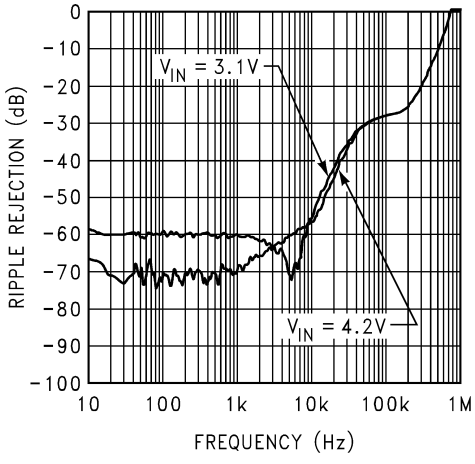
Dropout Voltage vs Load Current



20022229

Ripple Rejection ($C_{IN} = C_{OUT} = 1\mu F$, $I_L = 1mA$)



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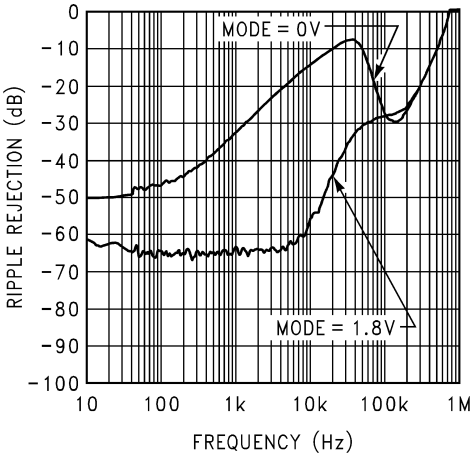
Ripple Rejection ($V_{IN} = V_{OUT(nom)} + 1V$, $C_{IN} = C_{OUT} = 1\mu F$, $I_L = 1mA$)



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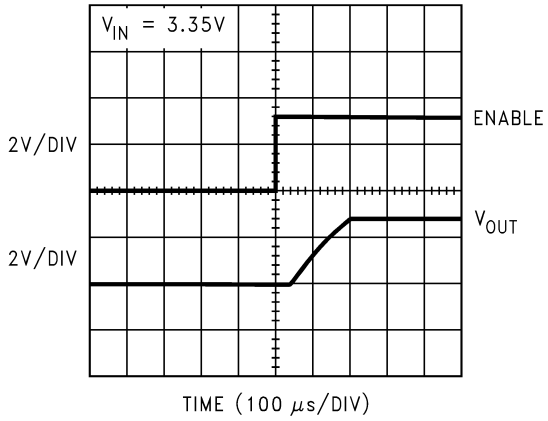
Typical Performance Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 1\ \mu F$ Ceramic, $V_{IN} = V_{OUT(nom)} + 0.5V$, $T_A = 25^{\circ}C$, Enable pin is tied to V_{IN}, MODE = 1.8V. (Continued)

T_{SLEEP} @ MODE = 0V, C_{OUT} = 1µF, I_L = 1mA



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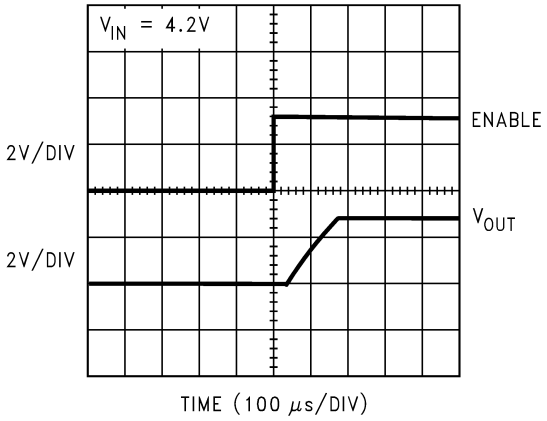
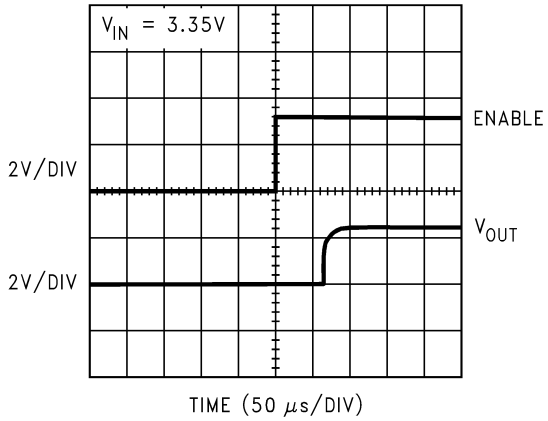
T_{SLEEP} @ MODE = 0V, C_{OUT} = 1µF, I_L = 1mA



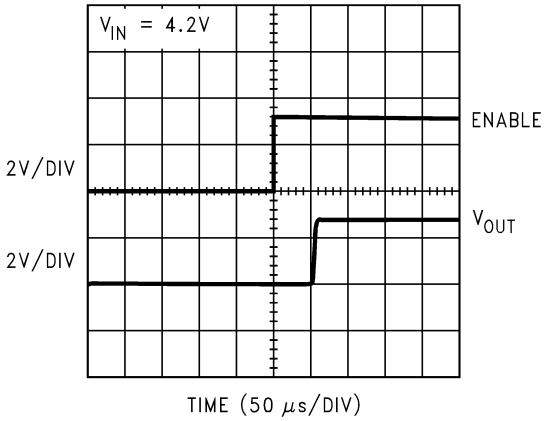
20022214

T_{ON} @ MODE = 1.8V, C_{OUT} = 1µF, I_L = 150mA



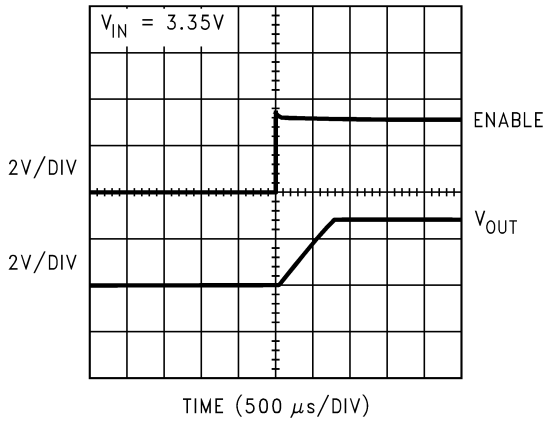
20022215

T_{ON} @ MODE = 1.8V, C_{OUT} = 1µF, I_L = 150mA



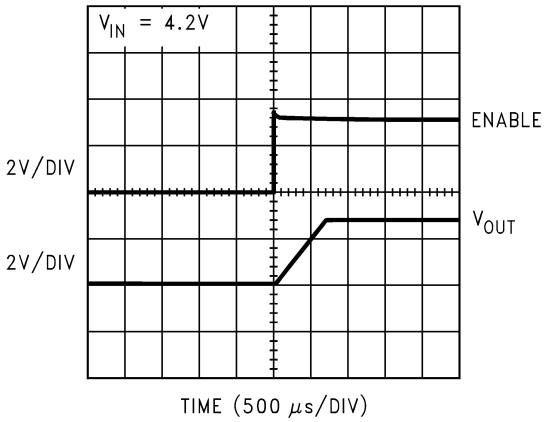
20022216

T_{SLEEP} @ MODE = 0V, C_{OUT} = 4.7µF, I_L = 1mA



20022217

T_{SLEEP} @ MODE = 0V, C_{OUT} = 4.7µF, I_L = 1mA

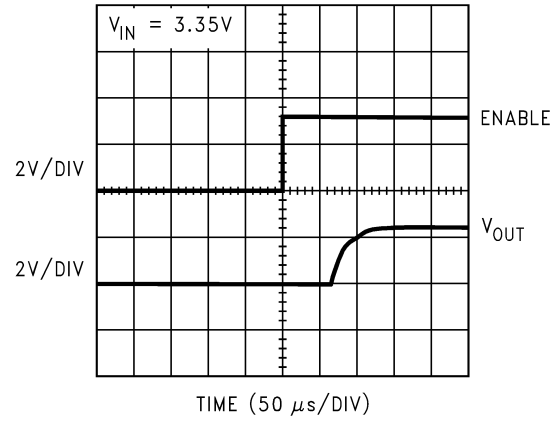


20022218

Typical Performance Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 1\ \mu F$ Ceramic, $V_{IN} = V_{OUT(nom)} + 0.5V$, $T_A = 25^{\circ}C$, Enable pin is tied to V_{IN}, MODE = 1.8V. (Continued)

T_{ON} @ MODE = 1.8V, C_{OUT} = 4.7µF, I_L = 150mA



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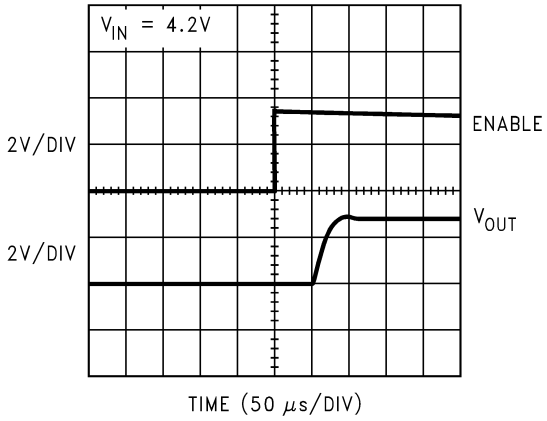
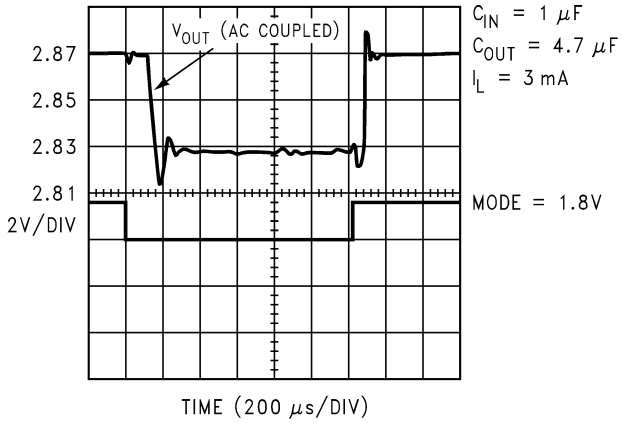
T_{ON} @ MODE = 1.8V, C_{OUT} = 4.7µF, I_L = 150mA



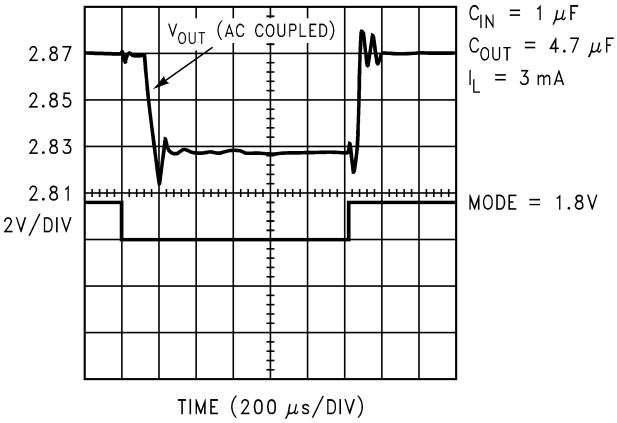
20022220

T_{MODE} Measurement @ V_{IN} = 3.05V



20022225

T_{MODE} Measurement @ V_{IN} = 3.6V



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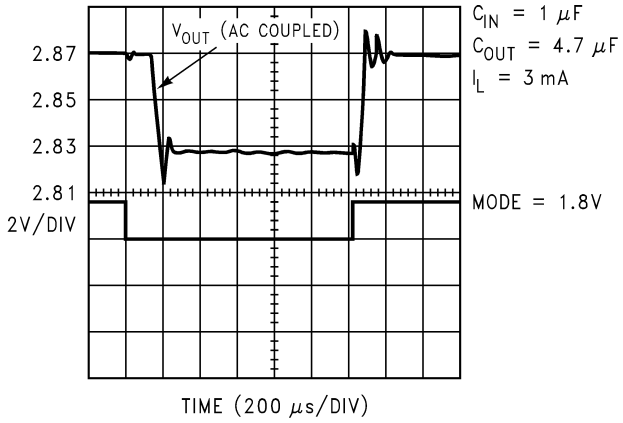
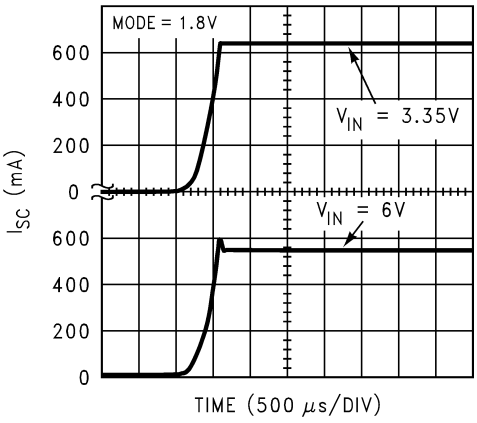
T_{MODE} Measurement @ V_{IN} = 4.2V



20022223

Output Short Circuit Current

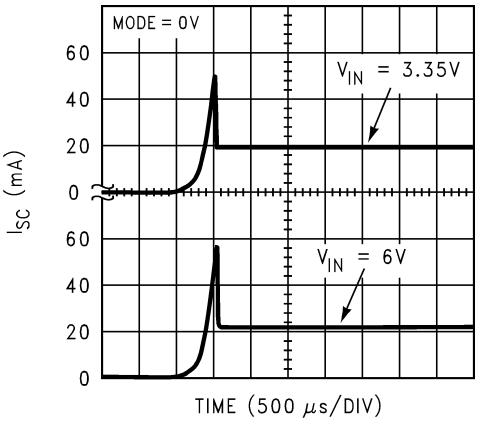


20022222

Typical Performance Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 1\ \mu F$ Ceramic, $V_{IN} = V_{OUT(nom)} + 0.5V$, $T_A = 25^{\circ}C$, Enable pin is tied to V_{IN}, MODE = 1.8V. (Continued)

Output Short Circuit Current



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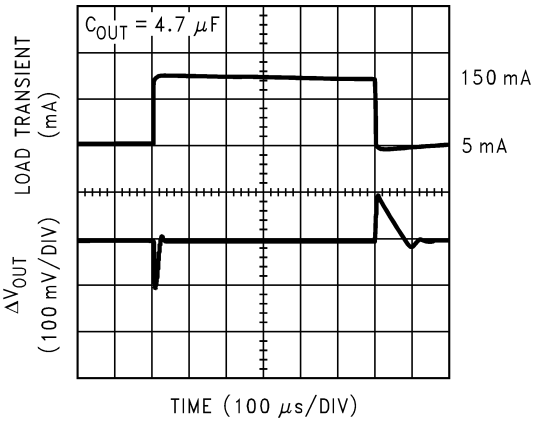
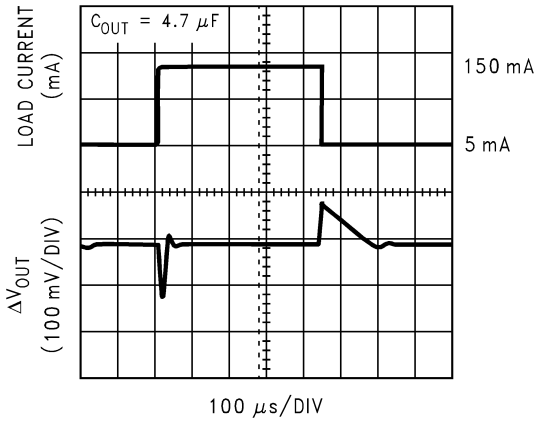
Load Transient Response @ V_{IN} = 3.1V



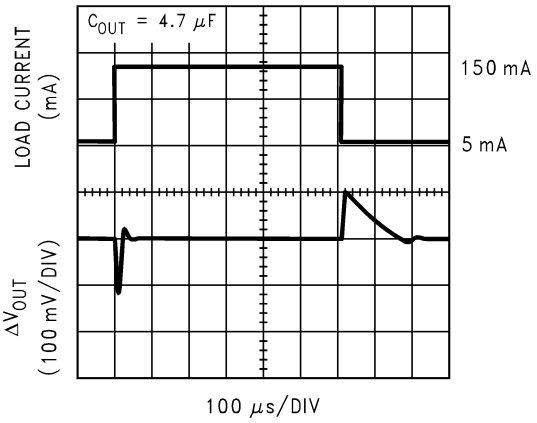
20022273

Load Transient Response @ V_{IN} = 3.35V



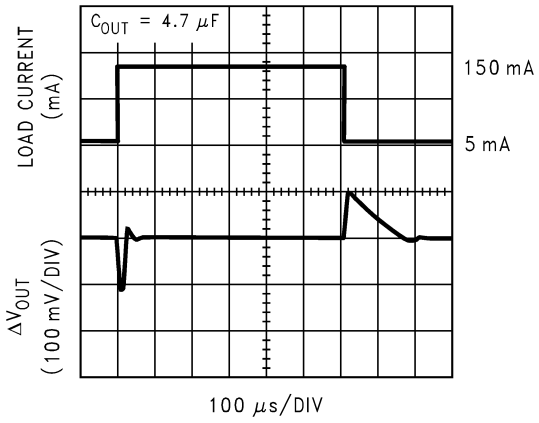
20022230

Load Transient Response @ V_{IN} = 3.6V



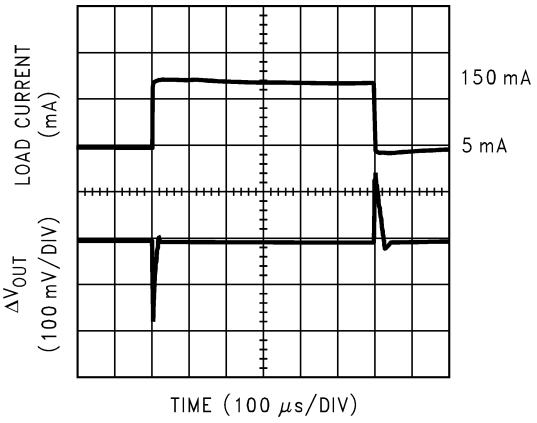
20022231

Load Transient Response @ V_{IN} = 4.2V



20022232

Load Transient Response @ V_{IN} = 3.1V, C_{OUT} = 1μF

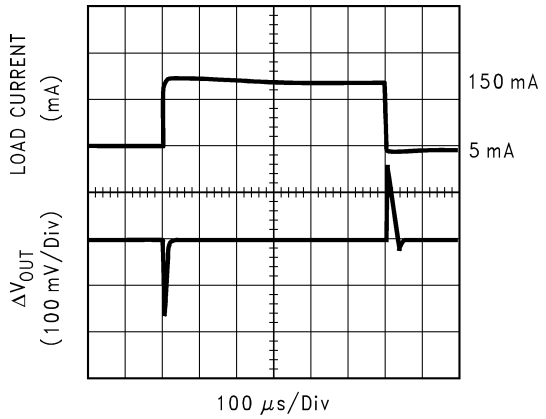


20022272

Typical Performance Characteristics

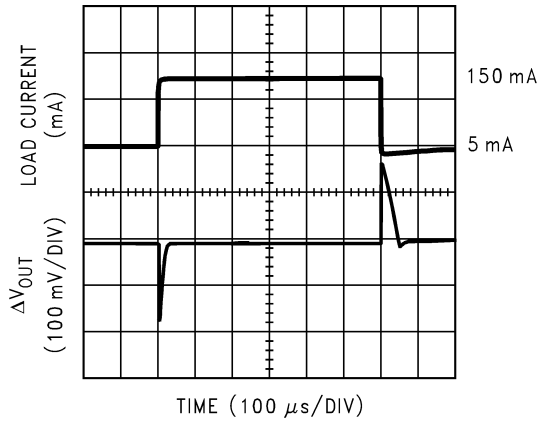
Unless otherwise specified, C_{IN} = C_{OUT} = 1 µF Ceramic, V_{IN} = $V_{OUT(nom)}$ + 0.5V, T_A = 25˚C, Enable pin is tied to V_{IN}, MODE = 1.8V. (Continued)

Load Transient Response @ V_{IN} = 3.35V, C_{OUT} = 1µF



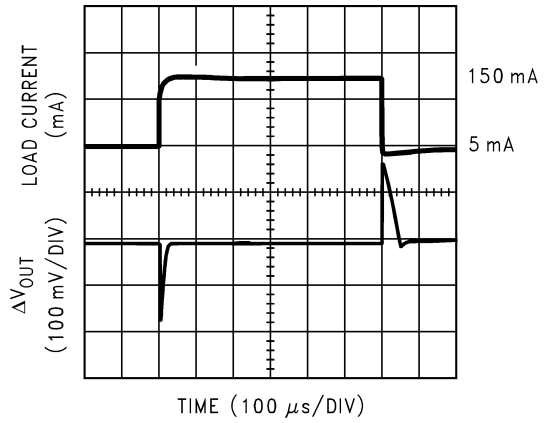
20022233

Load Transient Response @ V_{IN} = 4.2V, C_{OUT} = 1µF



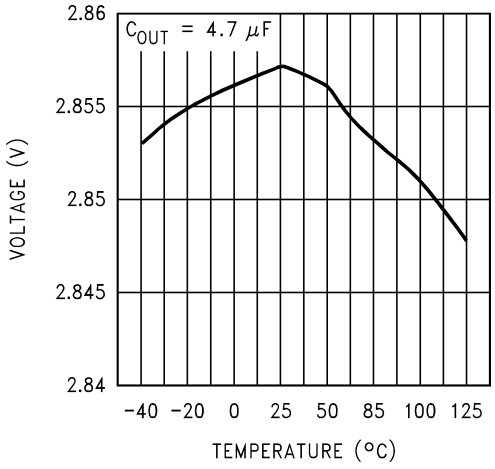
20022234

Load Transient Response @ V_{IN} = 3.6V, C_{OUT} = 1µF



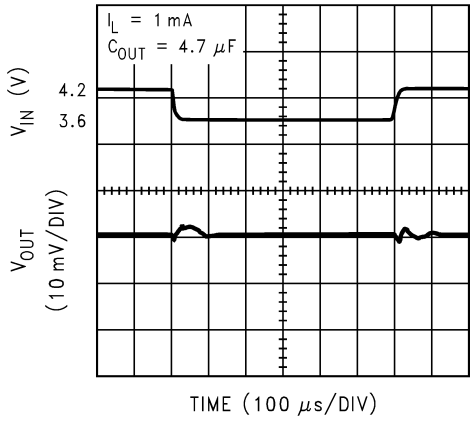
20022235

Output Voltage Change vs Temperature



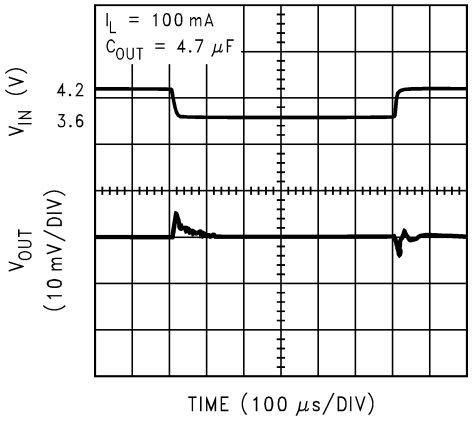
20022236

Line Transient Response



20022265

Line Transient Response

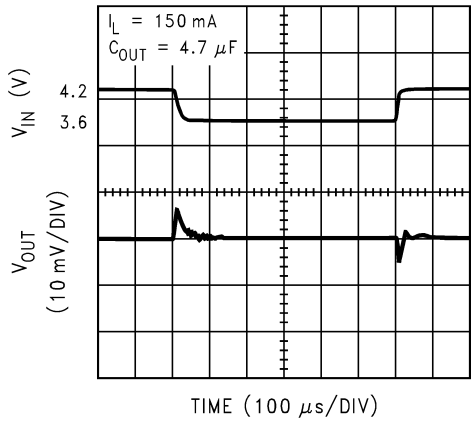


20022266

Typical Performance Characteristics

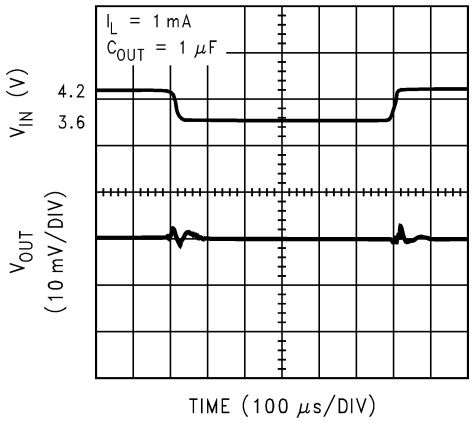
Unless otherwise specified, $C_{IN} = C_{OUT} = 1\ \mu F$ Ceramic, $V_{IN} = V_{OUT(nom)} + 0.5V$, $T_A = 25^{\circ}C$, Enable pin is tied to V_{IN}, MODE = 1.8V. (Continued)

Line Transient Response



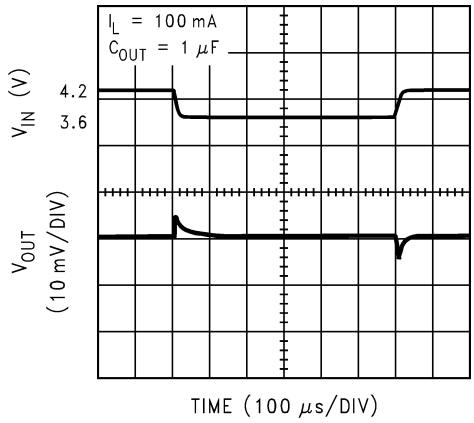
20022267

Line Transient Response



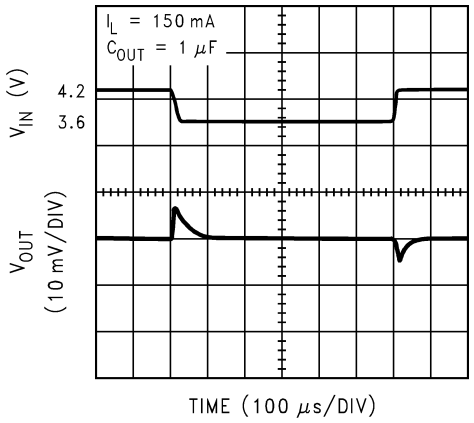
20022268

Line Transient Response



20022269

Line Transient Response



20022270

Application Hints

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP3987 requires external capacitors for regulator stability. The LP3987 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitance of ≅ 1µF is required between the LP3987 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be ≅ 1µF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP3987 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types Z5U, Y5V or X7R) in 1 to 4.7 µF range with 5mΩ to 500mΩ ESR range is suitable in the LP3987 application circuit.

It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see next section Capacitor Characteristics).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range (5 mΩ to 500 mΩ).

NO-LOAD STABILITY

The LP3987 will remain stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS

The LP3987 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 1µF to 4.7µF range, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability by the LP3987. The ceramic capacitor's capacitance can vary with temperature. Most large value ceramic capacitors (≅ 2.2µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25˚C to 85˚C.

A better choice for temperature coefficient in a ceramic capacitor is X7R, which holds the capacitance within ±15%. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25˚C down to –40˚C, so some guard band must be allowed.

ON/OFF INPUT OPERATION

The LP3987 is turned off by pulling the V_{EN} pin low, and turned on by pulling it high. If this feature is not used, the V_{EN} pin should be tied to V_{IN} to keep the regulator output on at all time. To assure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

MODE OPERATION

The LP3987 enters sleep mode by pulling MODE = 0V externally to reduce current during standby operation. During sleep mode, LP3987 consumes only 14µA of quiescent current and supplies up to 3mA of current. The device returns to active mode by pulling MODE = 1.8V. If this function is not used, the MODE pin should be tied to V_{IN}.

THERMAL PROTECTION

The LP3987 has internal thermal protection circuitry to disable the internal pass transistor if the junction temperature exceeds 125˚C to allow the device to cool down. The pass transistor will turn on when temperature falls below the maximum operating junction temperature of 125˚C. This feature is designed to protect the device in the event of fault conditions. For normal operation, it is suggested to limit the device junction temperature to less than 125˚C.

MICRO SMD MOUNTING

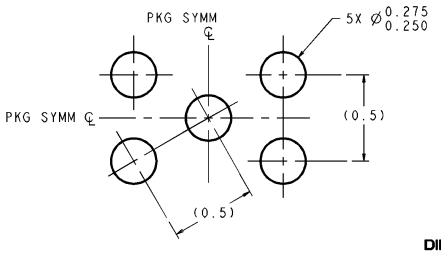
The micro SMD package requires specific mounting techniques which are detailed in National Semiconductor Application Note (AN-1112). Referring to the section *Surface Mount Technology (SMT) Assembly Considerations*, it should be noted that the pad style which must be used with the 5 pin package is NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the micro SMD device.

MICRO SMD LIGHT SENSITIVITY

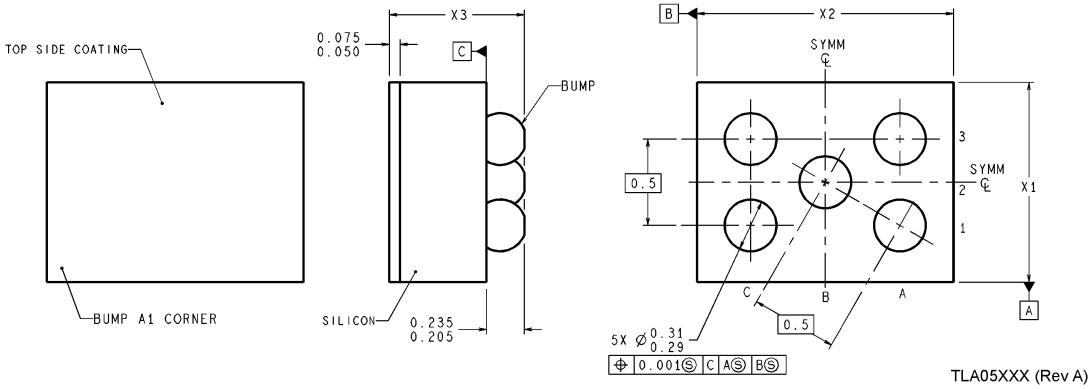
Exposing the micro SMD device to direct sunlight will cause misoperation of the device. Light sources such as Halogen lamps can effect electrical performance if brought near to the device. The wavelengths which have most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has very little effect on performance. A micro SMD test board was brought to within 1cm of a fluorescent desk lamp and the effect on the regulated output voltage was negligible, showing a deviation of less than 0.1% from nominal.

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

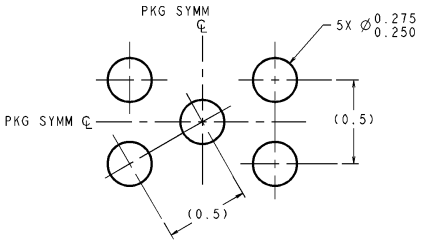
LAND PATTERN RECOMMENDATION



TLA05XXX (Rev A)

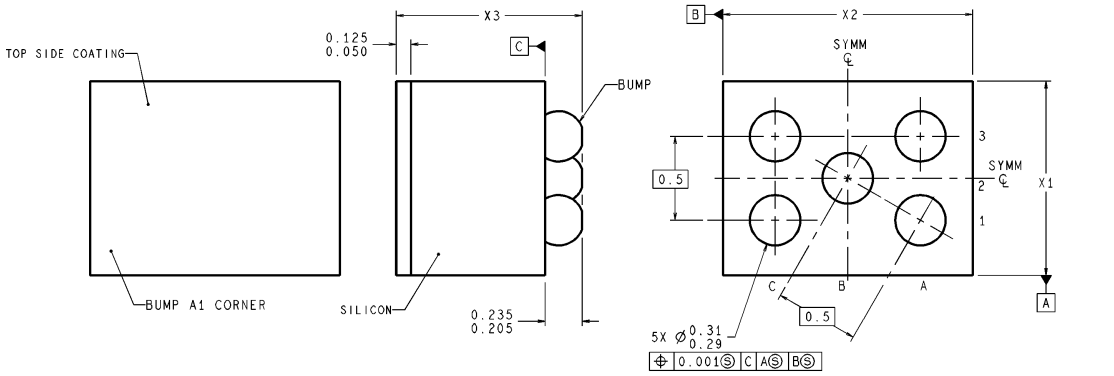
micro SMD, 5 Bump, Package (TLA05)
NS Package Number TLA05ADA
The dimensions for X1, X2 and X3 are given as:
X1 = 1.006 +/– 0.03mm
X2 = 1.438 +/– 0.03mm
X3 = 0.600 +/– 0.075mm

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

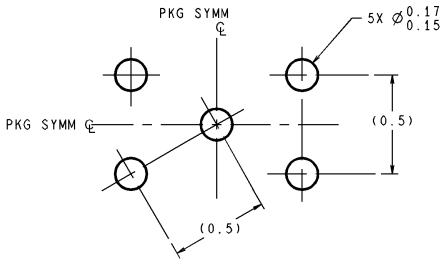
LAND PATTERN RECOMMENDATION



BLA05XXX (Rev C)

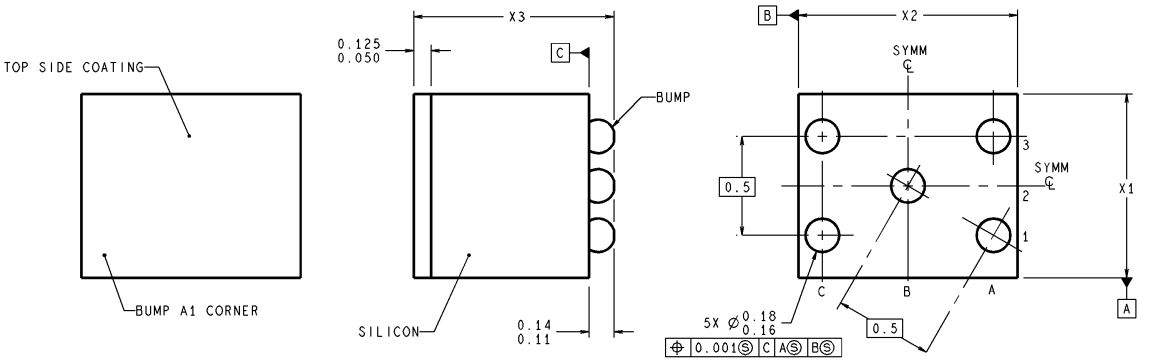
micro SMD, 5 Bump, Package (BLA05)
NS Package Number BLA05ADC
The dimensions for X1, X2 and X3 are given as:
X1 = 1.006 +/– 0.03mm
X2 = 1.438 +/– 0.03mm
X3 = 0.995 +/– 0.10mm

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

LAND PATTERN RECOMMENDATION



BPA05XXX (Rev C)

micro SMD, 5 Bump, Package (BPA05)
NS Package Number BPA05CMC
The dimensions for X1, X2 and X3 are given as:
X1 = 0.828 +/– 0.03mm
X2 = 1.387 +/– 0.03mm
X3 = 0.900 +/– 0.10mm

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