NCP100

Sub 1.0 V Precision Adjustable Shunt Regulator

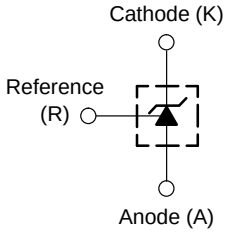
The NCP100 is a precision low voltage shunt regulator that is programmable over a voltage range of 0.9 V to 6.0 V. This device features a guaranteed reference accuracy of ±1.7% at 25°C and ±2.6% over the entire temperature range of –40°C to 85°C. The NCP100 exhibits a sharp low current turn–on characteristic with a low dynamic impedance of 0.20 Ω over an operating current range of 100 μA to 20 mA. These characteristics make this device an ideal replacement for zener diodes in numerous application circuits that require a precise low voltage reference. When combined with an optocoupler, the NCP100 can be used as an error amplifier for controlling the feedback loop in isolated low output voltage (2.3 V) switching power supplies. This device is available in an economical space saving TSOP–5 package.

Features

- Programmable Output Voltage Range of 0.9 V to 6.0 V
- Voltage Reference Tolerance of ±1.7%
- Sharp Low Current Turn–ON Characteristic
- Low Dynamic Output Impedance of 0.2 Ω from 100 μA to 20 mA
- Wide Operating Current Range of 80 μA to 20 mA
- Space Saving TSOP–5 Package

Applications

- Reference for Single Cell Alkaline, NiCD and NiMH Applications
- Low Output Voltage (2.3 V) Switching Power Supply Error Amp
- Battery Powered Consumer Products
- Portable Test Equipment and Instrumentation



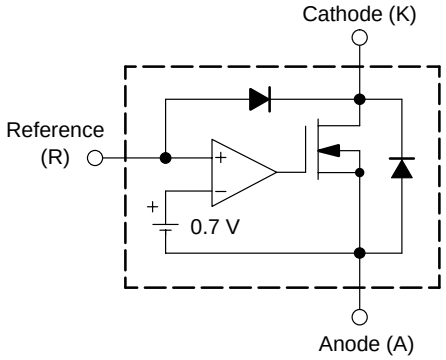


Figure 1. Symbol **Figure 2. Representative Block Diagram**

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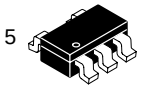
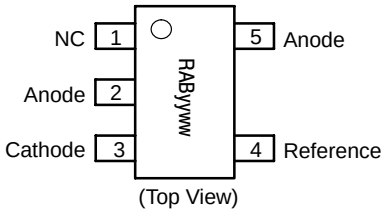


TSOP–5
SN SUFFIX
CASE 483

PIN CONNECTIONS AND MARKING DIAGRAM



YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NCP100SNT1	TSOP–5	3000 Units / 7″ Reel

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Cathode to Anode Voltage (Note 1)	V_{KA}	7.0	V
Cathode Current Range, Continuous (Note 2)	I_K	–20 to 25	mA
Reference Input Current Range, Continuous (Note 1)	I_{ref}	–0.05 to 2.0	mA
Thermal Resistance Junction to Air	$R_{\theta JA}$	225	°C/W
Operating Junction Temperature Range	T_J	–40 to 125	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	Min	Max	Unit
Cathode to Anode Voltage Range	V_{KA}	0.9	6.0	V
Cathode Current Range	I_K	0.1	20	mA

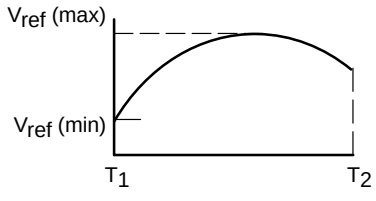
1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 4000 V per JESD–22, Method A114B.
   Machine Model Method 400 V.
2. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Reference Voltage (I_{KA} = 10 mA, Figure 3)	V_{ref}				V
V_{KA} = 0.9 V					
T_A = 25°C		0.684	0.696	0.708	
T_A = 0°C to 70°C		0.682	–	0.710	
T_A = –40°C to 85°C		0.678	–	0.714	
V_{KA} = 1.0 V					
T_A = 25°C		0.686	0.698	0.710	
T_A = 0°C to 70°C		0.684	–	0.712	
T_A = –40°C to 85°C		0.680	–	0.716	
Reference Input Voltage Change Over Temperature V_{KA} = 1.0 V, I_K = 10 mA, T_A = –40°C to 85°C, Figure 3 (Notes 3, 4)	ΔV_{ref}	–	1.0	12	mV
Reference Input Voltage Change Over Programmed Cathode Voltage (I_K = 10 mA, Figure 3)	Reg_{line}				mV
V_{KA} = 0.9 V to 1.0 V		–3.0	0.2	3.0	
V_{KA} = 1.0 V to 6.0 V		0	6.7	12	
Ratio of Reference Input Voltage Change to Cathode Voltage Change V_{KA} = 0.9 V to 6.0 V, I_K = 10 mA, Figure 3	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	–	1.3	2.4	mV/V
Reference Input Current (V_{KA} = 1.0 V, I_K = 10 mA)	I_{ref}	–100	–30	100	nA
Minimum Cathode Current for Regulation	$I_{K(min)}$	–	80	–	μA
Cathode Off–State Current (V_{KA} = 6.0 V, V_{ref} = 0 V)	$I_{K(off)}$	–	70	90	μA
Dynamic Output Impedance V_{KA} = 1.0 V, I_K = 100 μA to 20 mA, f ≤ 1.0 kHz, Figure 3	$\lvert Z_{KA} \rvert$	–	0.2	–	Ω

3. Low duty cycle pulse techniques are used during testing to maintain the junction temperatures as close to ambient as possible.
4. The ΔV_{ref} parameter is defined as the difference between the maximum and minimum values obtained over the ambient temperature range of –40°C to 85°C.



$\Delta V_{ref} = V_{ref}\,(max) - V_{ref}\,(min)$
$\Delta T_A = T_2 - T_1$

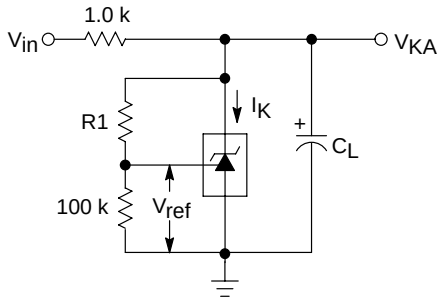


Figure 3. General Test Circuit

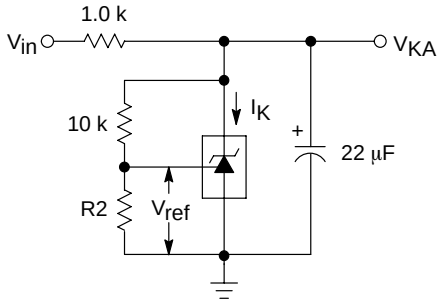


Figure 4. Test Circuit for Reference Input Voltage Change vs. Cathode Voltage

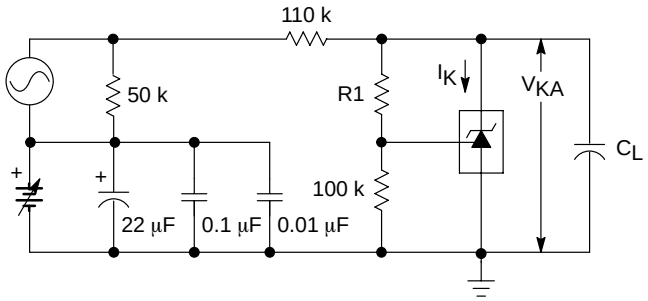


Figure 5. Test Circuit for Dynamic Impedance vs. Frequency

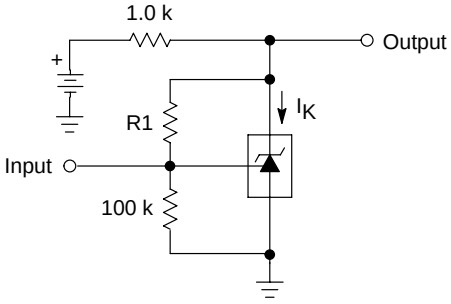


Figure 6. Test Circuit for Spectral Noise Density

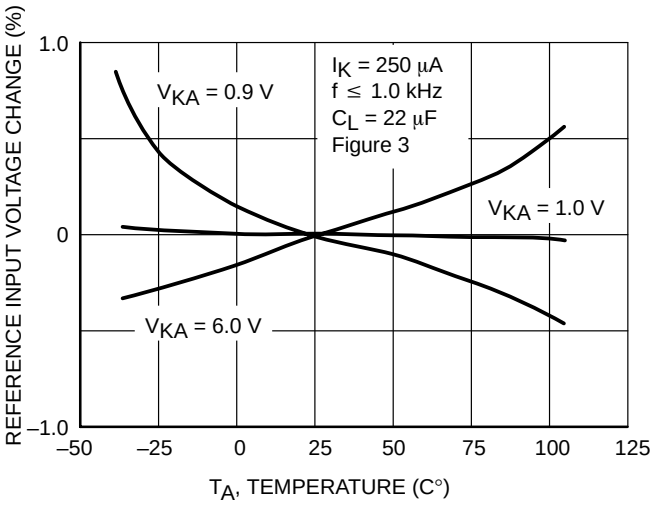


Figure 7. Reference Input Voltage Change vs. Ambient Temperature

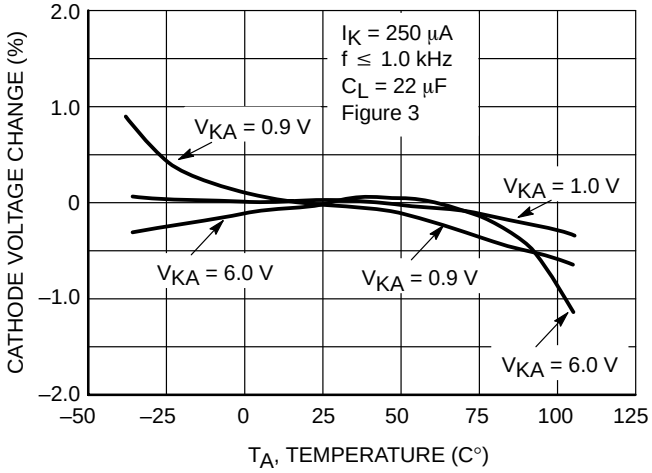


Figure 8. Cathode Voltage Change vs. Ambient Temperature

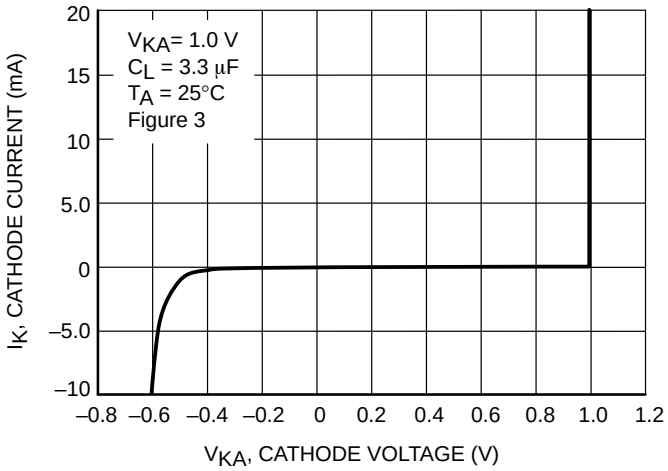


Figure 9. Cathode Current vs. Cathode Voltage

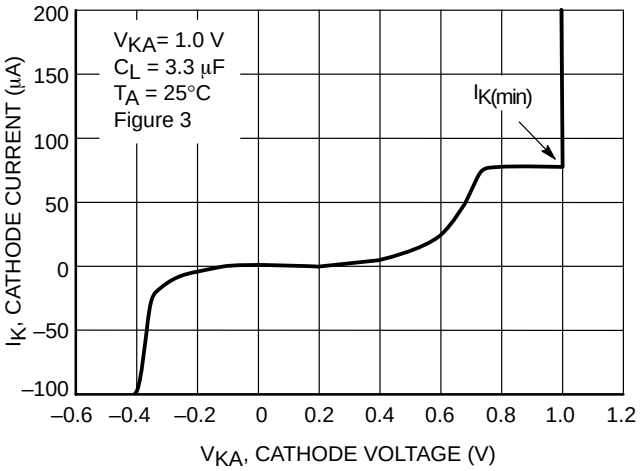


Figure 10. Cathode Current vs. Cathode Voltage

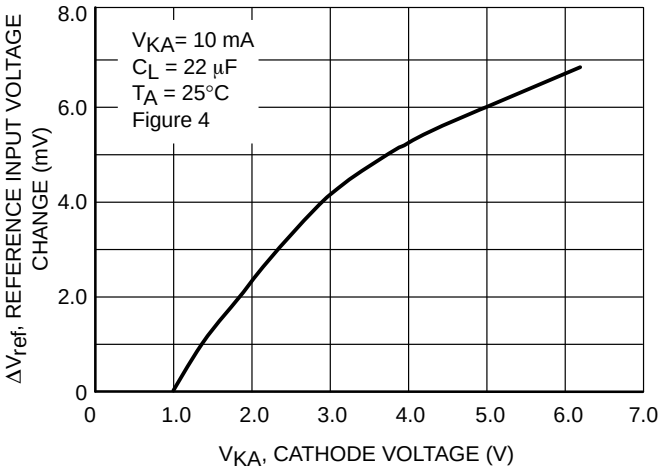


Figure 11. Reference Input Voltage Change vs. Cathode Voltage

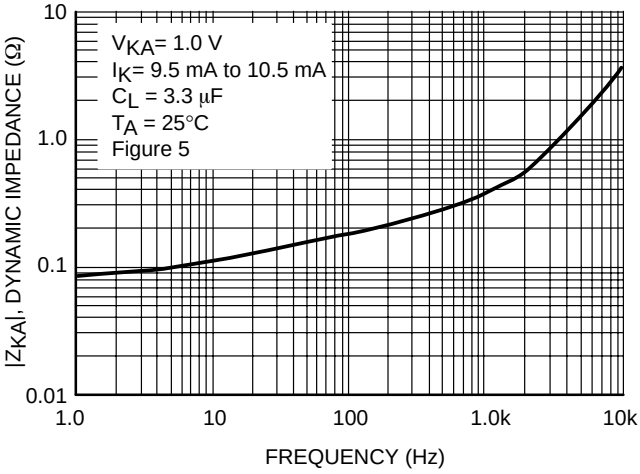


Figure 12. Dynamic Impedance vs. Frequency

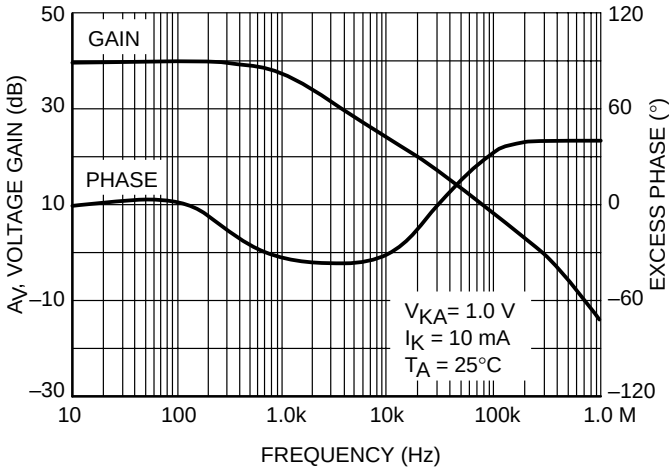


Figure 13. Small–Signal Voltage Gain and Phase vs. Frequency

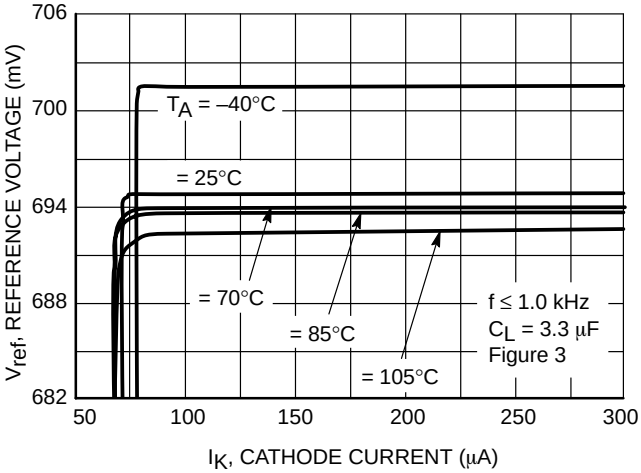


Figure 14. Reference Voltage vs. Cathode Current for V_{KA} = 0.9 V

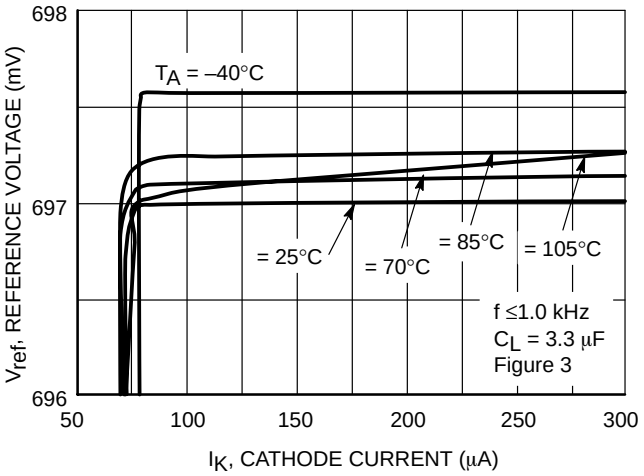


Figure 15. Reference Voltage vs. Cathode Current for V_{KA} = 1.0 V

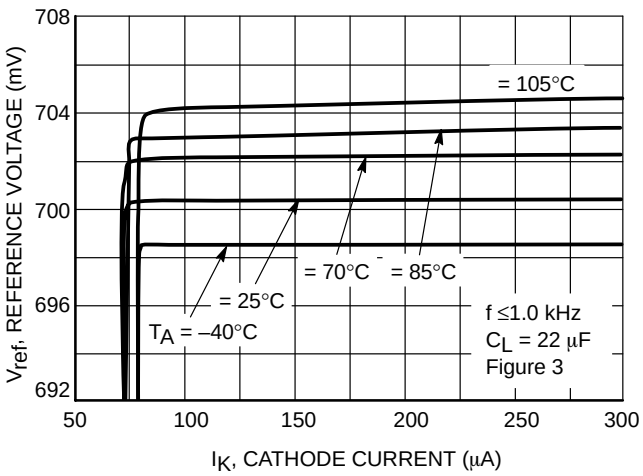


Figure 16. Reference Voltage vs. Cathode Current for V_{KA} = 6.0 V

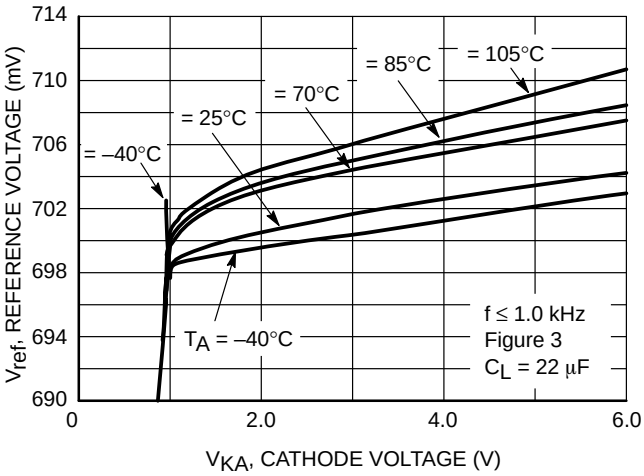


Figure 17. Reference Voltage vs. Cathode Current

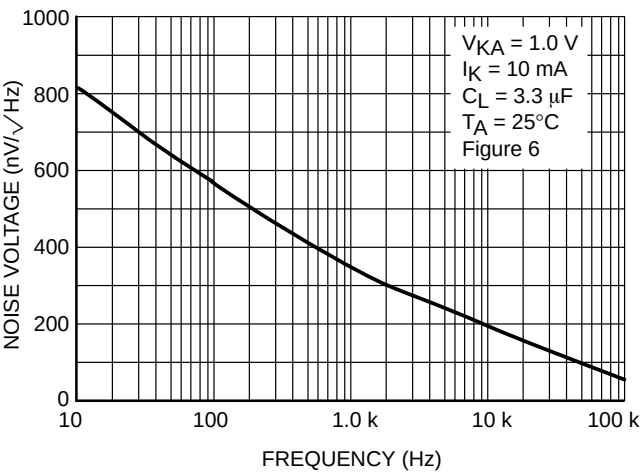


Figure 18. Spectral Noise Density

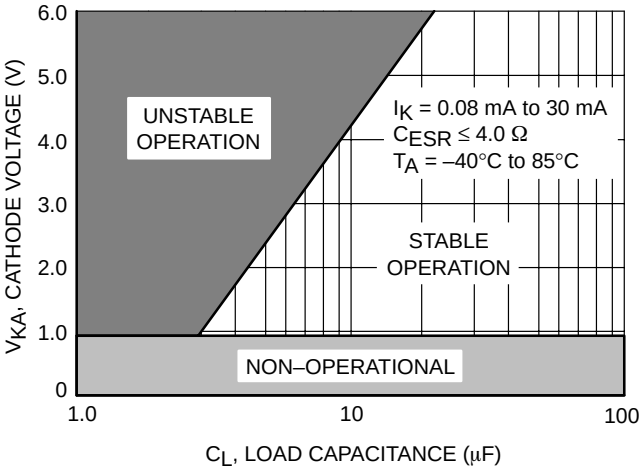


Figure 19. Stability Boundary Conditions

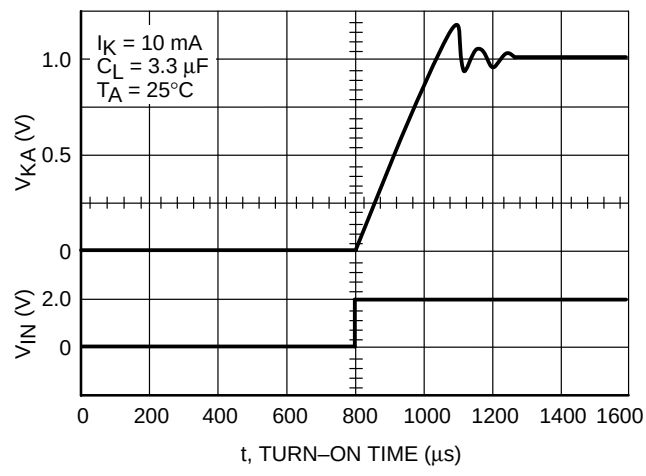


Figure 20. Turn–On Time

APPLICATIONS INFORMATION

The NCP100 is an adjustable shunt regulator similar to the industry standard 431–type regulators. Each device is laser trimmed at wafer probe to allow for tight reference accuracy and low reference voltage shift over the full operating temperature range of –40°C to 85°C (Figure 7).

The nominal value for the reference is 0.698 V. This lower voltage allows the device to be used in low voltage applications where the traditional 1.25 V and 2.5 V references are not suitable.

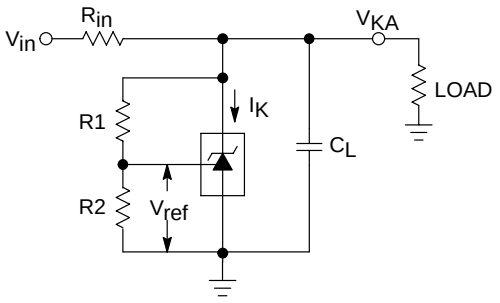


Figure 21. Typical Application Circuit

The typical application circuit for this device is shown in Figure 21. The cathode voltage can be programmed between 0.9 V to 6.0 V to allow for proper operation by setting the R1/R2 resistor divider network values. The following equation can be used in calculating the cathode voltage (V_{KA}). Note, if V_{KA} is known then the ratio of R1 and R2 can be determined from this equation as well.

$$V_{KA} = V_{ref}\left(1 + \frac{R1}{R2}\right) + I_{ref}\,R1$$

The table below shows the required R1/R2 values using 1.0% resistors for commonly used voltages.

V_{KA} (V)	R1 (kΩ)	R2 (kΩ)
0.9	30	100
1.0	43.2	100
1.8	158	100
3.3	374	100
5.0	619	100
6.0	750	100

Because the error amplifier is a CMOS design the value of I_{ref} is extremely low allowing it to be neglected for most applications. The low I_{ref} also allows for higher R1 and R2 values keeping current consumption very low.

The NCP100 is especially well suited for lower voltage applications, particularly at V_{KA} = 1.0 V. As is seen in Figures 7 and 8, this device exhibits excellent cathode and reference voltage flatness across the –40°C to 85°C temperature range.

In Figure 21, the input resistor (R_{in}) is nominally set to 1.0 kΩ. For proper operation, once V_{in}, R1 and R2 are set, the resistance and power value of R_{in} can be determined by the following equation.

$$R_{in} = \frac{V_{in} - V_{KA}}{I_K + I_L + \left(\frac{V_{KA}}{R_1 + R_2}\right)}$$

The maximum current that will flow through R_{in} must be determined. This is the sum of the maximum values of cathode current, resistor divider network current, and load current. With V_{in}, set, the difference (V_{in}–V_{KA}) is now constant. This value is divided by the maximum current calculated above to arrive at the value of R_{in}. Once the value of R_{in} is calculated, it's minimum power rating is easily derived by:

$$P_{in} = (I_{in})^2\,R_{in}$$

Once these values are determined, it should be verified that the minimum and maximum values of I_K are within the recommended range of 0.1 mA to 20 mA under the worst case conditions.

For stability, the NCP100 requires an output capacitor between the cathode and anode. Figure 19 shows the capacitance boundary values required for stable operation across the –40°C to 85°C temperature range. The goal is to remain to the right of the curve for any programmed cathode voltages. For example, if the V_{KA} is programmed to 1.0 V, then a load capacitor value of 3.0 μF or greater would be selected. The load capacitor's equivalent series resistance, ESR, should be less than 4.0 Ω. Both the capacitance and ESR values should be checked across the anticipated application temperature range to insure that the values meet the requirements stated above.

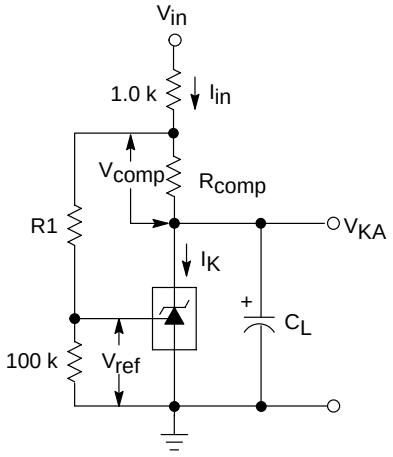


Figure 22. Negative Dynamic Impedance Circuit

One unique use for the NCP100 is that it can be configured for negative dynamic impedance as shown in Figure 22. This circuit is equivalent to Figure 21 with the addition of a small value resistor R_{comp} in the cathode circuit. The regulated voltage output remains across the NCP100 cathode and anode leads. The voltage programming and stability requirements remain the same as in the typical application shown in Figure 21.

The circuit performs the same as the one in Figure 21 with the exception of the effects of R_{comp}. As I_K increases, the voltage across R_{comp} also increases by:

$$V_{comp} = I_{KA} R_{comp}$$

V_{comp} effectively adjusts the NCP100 programmed V_{KA} voltage slightly down since the R1/R2 voltage divider will try to hold the point it is connected to at the programmed voltage. The regulator V_{KA} will now be lowered by the value of the V_{comp}. This effect can compensate for the NCP100's intrinsic positive impedance versus cathode current (I_K) to allow for 0 Ω or even a negative dynamic impedance.

Figure 23 shows this phenomenon for a program voltage of 1.0 V. The NCP100 intrinsic positive dynamic impedance response is the R_{comp} = 0 Ω curve. A 0 Ω dynamic impedance regulator response is realized with R_{comp} = 0.15 Ω. Negative dynamic impedance responses are achieved with R_{comp} > 0.15 Ω.

Figure 24 shows the characteristic at a programmed V_{KA} of 6.0 V. The 0 Ω dynamic impedance value corresponds to R_{comp} = 2.9 Ω.

Figure 25 shows the dynamic impedance versus cathode compensation resistance for programmed voltages of 1.0 V, 3.3 V and 6.0 V. It can be seen that any value up to the positive intrinsic dynamic impedance of the NCP100 can be realized. The other limit is that with a high enough negative dynamic impedance, the NCP100 V may drop below the minimum operating V_{KA} voltage of 0.9 V, which can result in unpredictable performance.

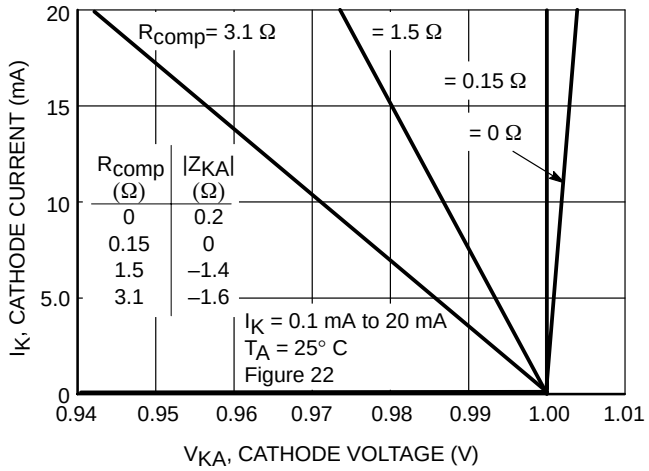


Figure 23. Cathode Current vs. Cathode Voltage for Programmed V_{KA} = 1.0 V

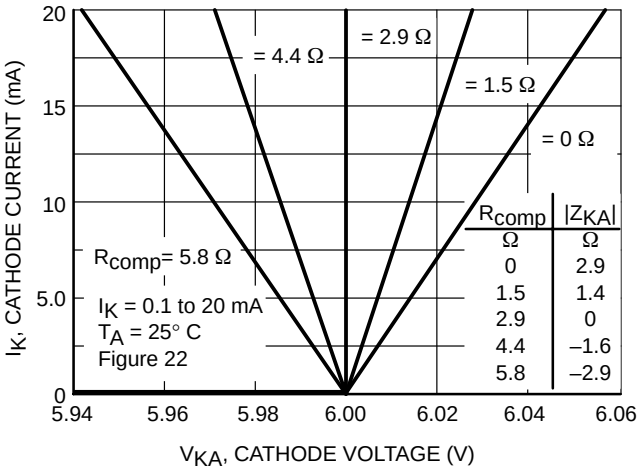


Figure 24. Cathode Current vs. Cathode Voltage for Programmed V_{KA} = 6.0 V

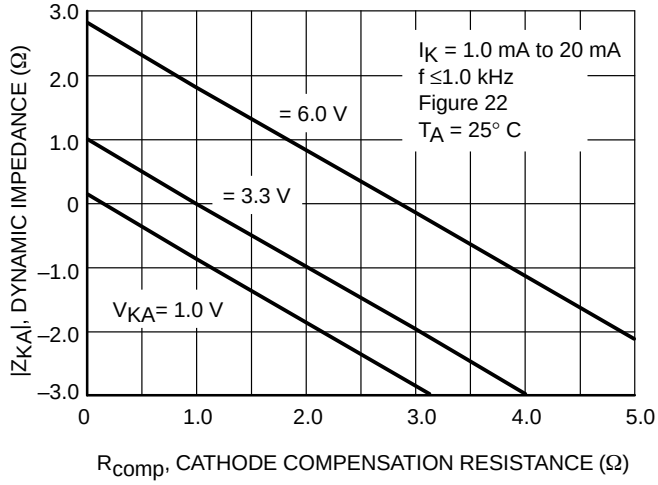


Figure 25. Dynamic Impedance vs. Cathode Compensation Resistance

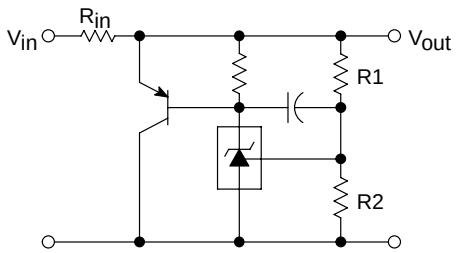


Figure 26. High Current Shunt Regulator

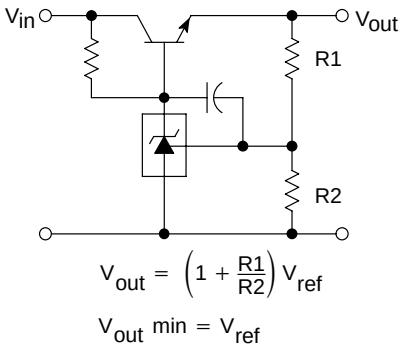


Figure 27. Low Dropout Series Pass Regulator

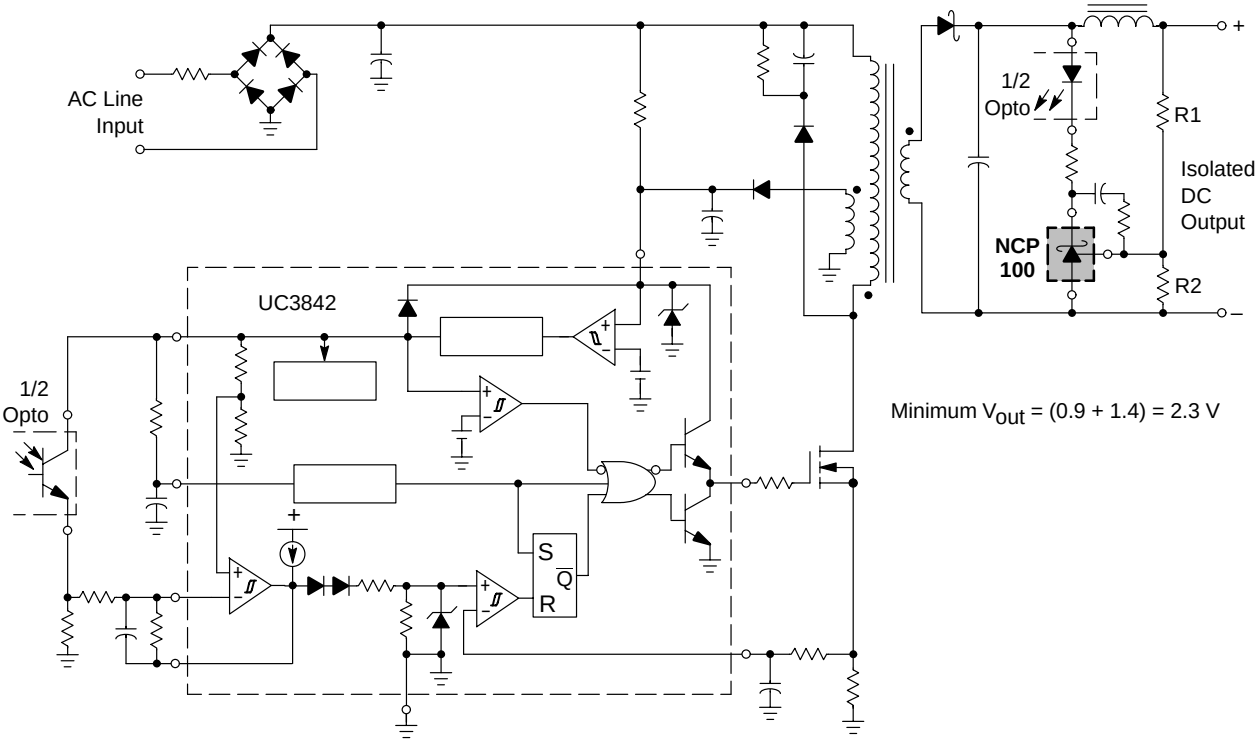


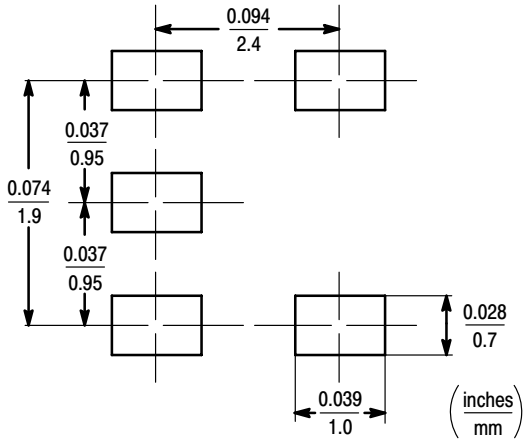
Figure 28. Offline Converter with Isolated DC Output

The circuit in Figure 28 uses the NCP100 as a compensated amplifier for controlling the feedback loop of an isolated output line powered converter. This device allows the converter to directly regulate the output voltage at a significantly lower level than obtainable with the common TL431 device family. The output voltage is programmed by the resistors R1 and R2. The minimum regulated DC output is limited to the sum of the lowest allowable cathode to anode voltage (0.9 V) and the forward drop of the optocoupler light emitting diode (1.4 V).

INFORMATION FOR USING THE TSOP–5 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

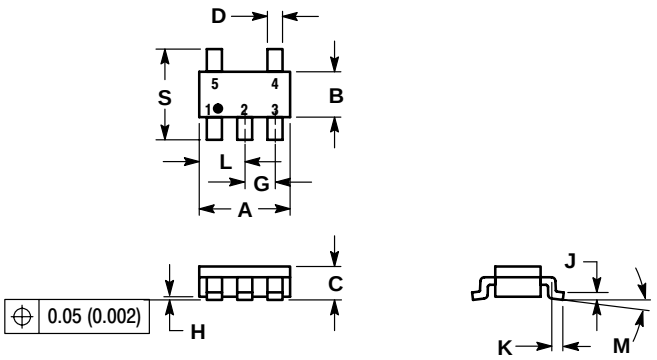
Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



TSOP–5

PACKAGE DIMENSIONS

TSOP–5
SN SUFFIX
PLASTIC PACKAGE
CASE 483–01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181

Notes

PUBLICATION ORDERING INFORMATION

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