Single Non-Inverting Buffer with Open Drain Output

The MC74VHC1G07 is an advanced high speed CMOS buffer with open drain output fabricated with silicon gate CMOS technology.

The internal circuit is composed of multiple stages, including a buffer and an open drain output which provides the capability to set the output switching level. This allows the MC74VHC1G07 to be used to interface any 2.0 V to 5.5 V circuit to circuits of any voltage between 1.5 V and 7 V using an external resistor and power supply.

The MC74VHC1G07 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage.

- High Speed: $t_{PD} = 3.8 \text{ ns}$ (Typ) at $V_{CC} = 5 \text{ V}$
- Low Internal Power Dissipation: $I_{CC} = 1 \mu A \text{ (Max)}$ at $T_A = 25 \text{°C}$
- Power Down Protection Provided on Inputs
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 105

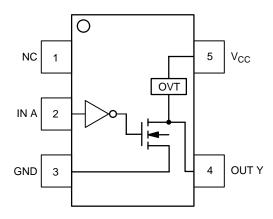


Figure 1. Pinout



Figure 2. Logic Symbol



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SC70-5/SC-88A/SOT-353 DF SUFFIX CASE 419A



MARKING

Pin 1



SOT23-5/TSOP-5/SC59-5 DT SUFFIX CASE 483



d = Date Code

	PIN ASSIGNMENT						
1	NC						
2	IN A						
3	GND						
4	OUT Y						
5	V _{CC}						

FUNCTION TABLE

A Input	Y Output
L	L
Н	Z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

Symbol		Value	Unit	
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V	
V _{IN}	DC Input Voltage	-0.5 to +7.0	V	
V _{OUT}	DC Output Voltage		-0.5 to +7.0	V
I _{IK}	DC Input Diode Current		-20	mA
I _{OK}	DC Output Diode Current	$V_{OUT} < GND; V_{OUT} > V_{CC}$	+20	mA
I _{OUT}	DC Output Sink Current, per Pin		+ 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND F	Pin	+50	mA
T _{STG}	Storage Temperature Range		-65 to +150	°C
TL	Lead Temperature, 1 mm from Case	260	°C	
TJ	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance	SC70-5/SC-88A/SOT-353 (Note 1) SOT23-5/TSOP-5/SC59-5	350 230	°C/W
P _D	Power Dissipation in Still Air at 85°C	SC70-5/SC-88A/SOT-353 SOT23-5/TSOP-5/SC59-5	150 200	mW
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>2000 >200 N/A	V
I _{LATCH-UP}	Latch-Up Performance	Above V _{CC} and Below GND at 125°C (Note 5)	±500	mA

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute—maximum—rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

- 1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
- 2. Tested to EIA/JESD22-A114-A.
- 3. Tested to EIA/JESD22-A115-A.
- 4. Tested to JESD22-C101-A.
- 5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage		2.0	5.5	V
V _{IN}	DC Input Voltage		0.0	5.5	V
V _{OUT}	DC Output Voltage		0.0	7.0	V
T _A	Operating Temperature Range		- 55	+125	°C
t _r , t _f	Input Rise and Fall Time	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0 0	100 20	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

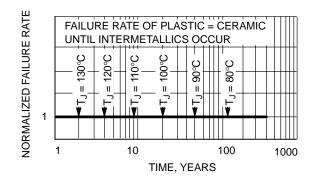


Figure 3. Failure Rate vs. Time Junction Temperature

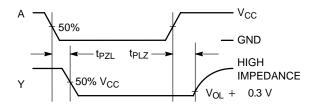
DC ELECTRICAL CHARACTERISTICS

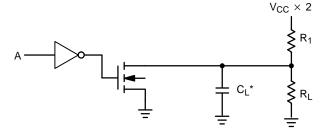
			V _{CC}	-	T _A = 25°	С	T _A ≤	85°C	-55°C ≤ 1	T _A ≤ 125°C	
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V _{IL}	Maximum Low-Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V _{OL}	Maximum Low-Level Output Voltage	$V_{IN} = V_{IL}$ $I_{OL} = 50 \mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
	$V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IL}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I _{LKG}	Z-State Output Leakage Current	$V_{IN} = V_{IH}$ $V_{OUT} = V_{CC}$ or GND	5.5			± 0.25		± 2.5		±5.0	μΑ
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			± 0.1		±1.0		±1.0	μΑ
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1.0		20		40	μΑ
I _{OFF}	Power Off–Output Leakage Current	V _{OUT} = 5.5 V V _{IN} = 5.5 V	0			0.25		2.5		5	μΑ

AC ELECTRICAL CHARACTERISTICS Input $t_f = t_f = 3.0 \text{ ns}$

			1	$T_A = 25^{\circ}C$		T _A ≤	$T_A \le 85^{\circ}C$ $-55^{\circ}C \le T_A \le 125^{\circ}C$			
Symbol	Parameter	Test Conditions	Min	Тур	Max	Min	Max	Min	Max	Unit
t _{PZL}	Maximum Output Enable Time, Input A to \overline{Y}	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $C_L = 15 \text{ pF}$ $R_L = R_I = 500 \Omega$ $C_L = 50 \text{ pF}$		5.0 7.5	7.1 10.6		8.5 12.0		10.0 14.5	ns
		$\begin{array}{cccccccccccccccccccccccccccccccccccc$		3.8 5.3	5.5 7.5		6.5 8.5		8.0 10.0	
t _{PLZ}	Maximum Output Disable Time	$\begin{array}{c} \text{V}_{\text{CC}} = 3.3 \pm 0.3 \text{V} \text{C}_{\text{L}} = 50 \text{pF} \\ \text{R}_{\text{L}} = \text{R}_{\text{I}} = 500 \Omega \end{array}$		7.5	10.6		12.0		14.5	ns
		$V_{CC} = 5.0 \pm 0.5 \text{ V}$ $C_L = 50 \text{ pF}$ $R_L = R_I = 500 \Omega$		5.3	7.5		8.5		10.0	
C _{IN}	Maximum Input Capacitance			4	10		10		10	pF
							ypical @	25°C, V _{CC} =	= 5.0 V	
C_{PD}	C _{PD} Power Dissipation Capacitance (Note 6)							18		рF

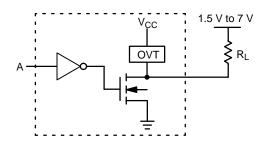
^{6.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no–load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.





*Includes jig and probe capacitance. $R_L = R_1 = 500 \ \Omega$

Figure 4. Switching Waveforms



g Waveforms Figure 5. Test Circuit

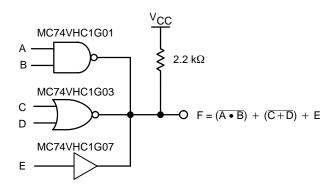


Figure 6. Output Voltage Mismatch Application

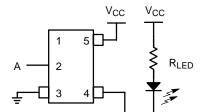


Figure 8. LED Driver

Figure 7. Complex Boolean Functions

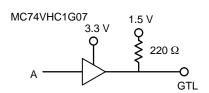


Figure 9. GTL Driver

DEVICE ORDERING INFORMATION

		Device Nomenclature						
Device Order Number	Logic Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape and Reel Suffix	Package Type (Name/SOT#/ Common Name)	Tape and Reel Size [†]
MC74VHC1G07DFT1	MC	74	VHC1G	07	DF	T1	SC70-5/SC-88A/ SOT-353	178 mm (7 in) 3000 Unit
MC74VHC1G07DFT2	MC	74	VHC1G	07	DF	T2	SC70-5/SC-88A/ SOT-353	178 mm (7 in) 3000 Unit
MC74VHC1G07DTT1	MC	74	VHC1G	07	DT	T1	SOT23-5/TSOP-5/ SC59-5	178 mm (7 in) 3000 Unit

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

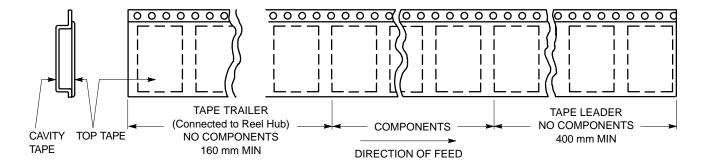


Figure 10. Tape Ends for Finished Goods

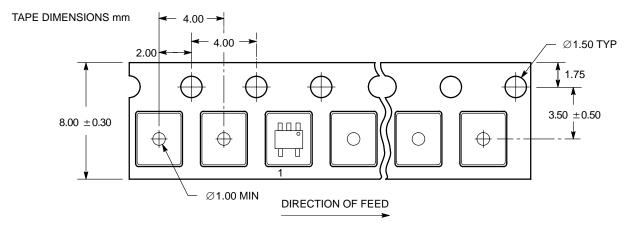


Figure 11. SC-70-5/SC-88A/SOT-353 DFT1 Reel Configuration/Orientation

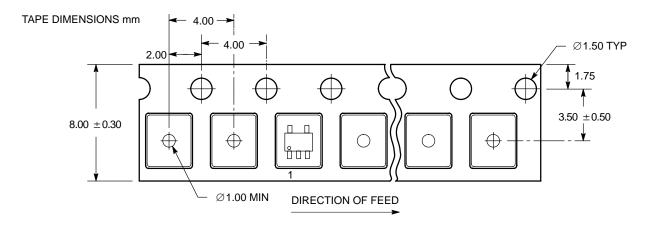


Figure 12. SC-70/SC-88A/SOT-353 DFT2 and SOT23-5/TSOP-5/SC59-5 DTT1 Reel Configuration/Orientation

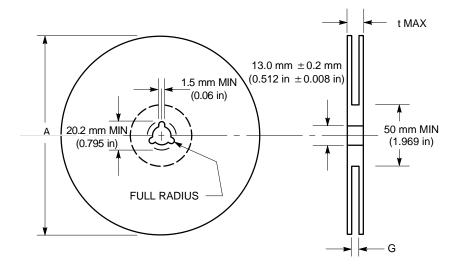


Figure 13. Reel Dimensions

REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7 in)	8.4 mm, + 1.5 mm, -0.0 (0.33 in + 0.059 in, -0.00)	14.4 mm (0.56 in)

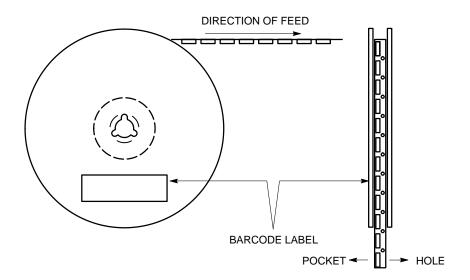
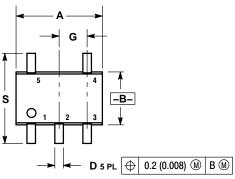


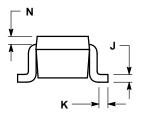
Figure 14. Reel Winding Direction

PACKAGE DIMENSIONS

SC70-5/SC-88A/SOT-353 **DF SUFFIX**

5-LEAD PACKAGE CASE 419A-02 ISSUE G





- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. 419A-01 OBSOLETE. NEW STANDARD

- 419A-02.
 DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INC	HES	MILLIM	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.071	0.087	1.80	2.20
В	0.045	0.053	1.15	1.35
С	0.031	0.031 0.043 0.80		1.10
D	0.004	0.012	0.10	0.30
G	0.026	BSC	0.65	BSC
Н		0.004	-	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008	0.008 REF		REF
S	0.079	0.087	2.00	2.20

SOLDERING FOOTPRINT*

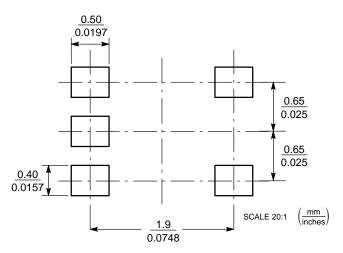


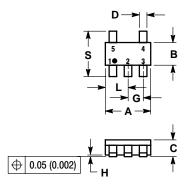
Figure 15. SC-88A/SC70-5/SOT-353

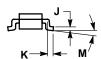
^{*}For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOT23-5/TSOP-5/SC59-5 **DT SUFFIX**

5-LEAD PACKAGE CASE 483-01 ISSUE C





NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- ANSI 114-3M, 1992.
 CONTROLLING DIMENSION: MILLIMETER.
 MAXIMUM LEAD THICKNESS INCLUDES
 LEAD FINISH THICKNESS. MINIMUM LEAD
 THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
- A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	2.90	3.10	0.1142	0.1220	
В	1.30	1.70	0.0512	0.0669	
С	0.90	1.10	0.0354	0.0433	
D	0.25	0.50	0.0098	0.0197	
G	0.85	1.05	0.0335	0.0413	
Н	0.013	0.100	0.0005	0.0040	
J	0.10	0.26	0.0040	0.0102	
K	0.20	0.60	0.0079	0.0236	
L	1.25	1.55	0.0493	0.0610	
М	0	10	0	10	
S	2.50	3.00	0.0985	0.1181	

SOLDERING FOOTPRINT*

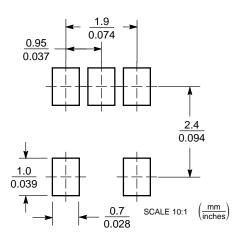


Figure 16. THIN SOT23-5/TSOP-5/SC59-5

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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