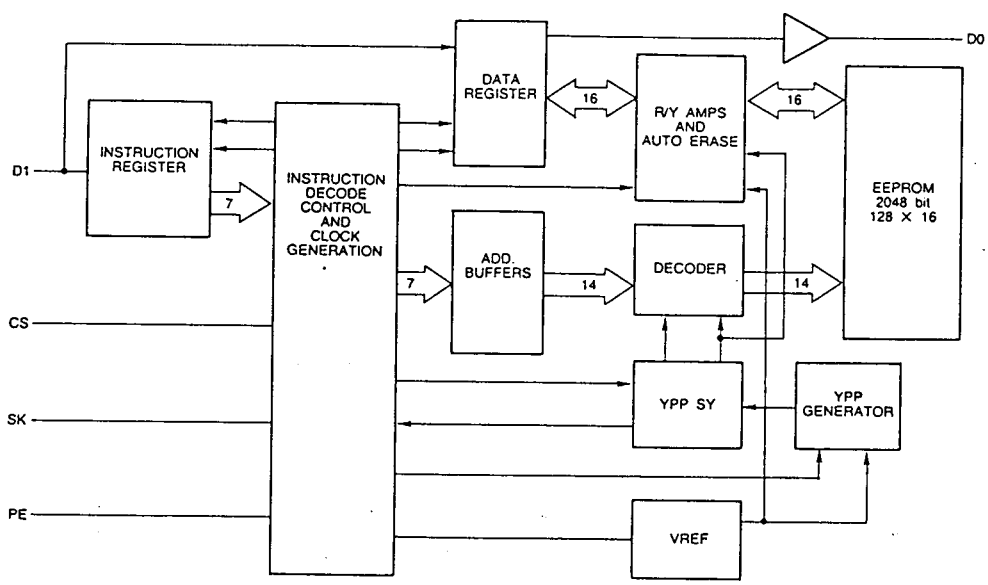
AK93C57 Series

PRELIMINARY

Wide Vcc (2.5V ~ 5.5V) 2048 bit Serial Electrically Erasable PROM

FEATURES

■ADVANCED CMOS E^2PROM TECHNOLOGY
■READ/WRITE NON-VOLATILE MEMORY
—Wide Vcc (2.5V ~ 5.5V) operation
—2048 bits, 128 × 16 organization
—Easy to use yet versatile serial data interface
■LOW POWER CONSUMPTION
—5mA Max Active
—1mA Max Standby, TTL interface
—100 µA Max Standby, CMOS interface
■SPECIAL FEATURES
—Automatic write cycle time-out with auto-ERASE
—Ready/Busy status signal
—Software and Hardware controlled write protection
■IDEAL FOR LOW DENSITY DATA STORAGE
—Low cost, space saving, 8-pin package
—Interfaces with popular microcontrollers and standard microprocessors
■APPLICATION VERSATILITY
—Alarm Devices, Electronic Locks, Appliances, Terminals, Smart Cards, Satellite Receivers, Meters, Telephones, Tuners, etc.



Block Diagram

GENERAL DESCRIPTION

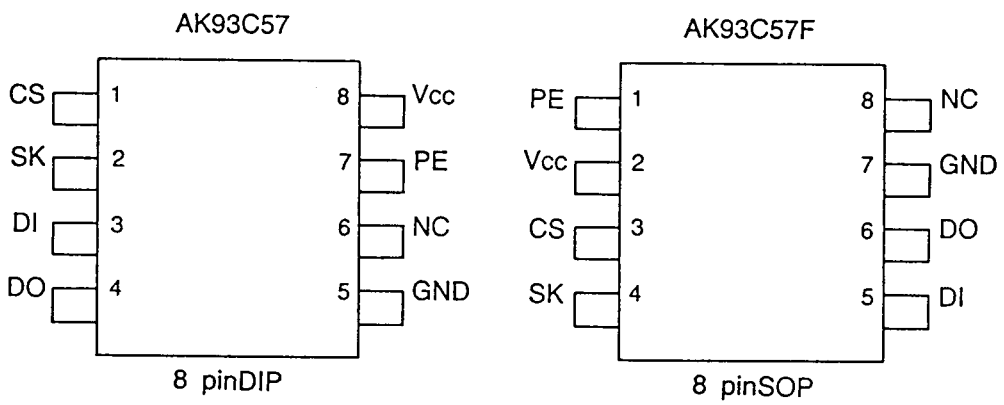
The AK93C57 is a 2048-bit, serial, read/write, non-volatile memory device fabricated using an advanced CMOS E²PROM technology. Its 2048 bits of memory are organized into 128 registers of 16 bits each. It can operate full function under wide operating voltage range from 2.5V to 5.5V.
Each register is individually addressable for serial read or write operations. A versatile serial interface, consisting of chip select, clock, program enable, data-in and data-out, can easily be controlled by popular microcontrollers or standard microprocessors.

Low power consumption, low cost, and space efficiency make the AK93C57 an ideal candidate for high volume, low density, data storage applications. Special features of the AK93C57 include: automatic write time-out with auto-ERASE, ready/busy status signal, software and hardware controlled write protection and ultra-low standby power mode when deselected (CS=low).

■Product Selection Guide

Model	Temp. Range	Vcc	Package
AK93C57	0°C ~ 70°C	2.5V ~ 5.5V	8 pin Plastic DIP
AK93C57F	0°C ~ 70°C	2.5V ~ 5.5V	8 pin Plastic SOP

■Pin Configuration



CS = Chip Select
SK = Serial Clock
PE = Program Enable
DI = Serial Data Input
DO = Serial Data Output
GND = Ground
Vcc = Power Supply
NC = Not Connected

FUNCTIONAL DESCRIPTION

Device Operation

The AK93C57 is a serial 2048 bit peripheral memory device intended for use in non-volatile data storage applications. Its memory organization consists of 128 registers, each 16-bits wide. Each register is independently addressable for read or write operations.

Five 11-bit serial instructions are used to control the operation of the AK93C57. These instructions are serially clocked into the DI input as controlled by the CS, PE and SK input. The instructions include read, erase/write enable, erase/write disable, write and write all. The format of each instruction has a logical "01" as a start bit, two bits as an opcode, and 7 bits of address. During read operations the DO output is valid as data out after the address is entered. PE (Program Enable) input prevents any accidental programming. PE must be kept high during entering instructions of WRITE and WRAL. After a write instruction, the DO output serves as a ready/busy status indicator signaling when the operation is complete allowing further read or write access. The ready/busy status indicator is only valid when CS is active (high). When CS is low, the DO output goes into a high impedance state. After a new instruction is initiated, the DO output also goes to high impedance.

CS must be brought low for a minimum of 250ns (Tcs) between consecutive instruction cycles.

During a programming mode (WRITE, WRAL), SK clock is only needed while the actual instruction, i.e. start bit, op-code address and data is being input. It can remain deactivated during the self-timed programming cycle and status check.

Read

The read instruction is the only instruction which outputs serial data on the DO pin. After a read instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out-shift register. A dummy bit (logical "0") precedes the 16-bit data output string. The output data changes during the high states of the system clock.

Erase/Write Enable and Disable

When Vcc is applied to the part it powers up in the programming disable (EWDS) state. Programming must be preceded by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or Vcc is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is independent of both EWEN and EWDS instructions.

Write

The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data in (DI) pin, CS must be brought low before the next rising edge of the SK clock. PE must be kept high during entering the instruction. This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 250ns (Tcs). DO= logical "0" indicates that programming is still in progress. DO= logical "1" indicates that the register at the address specified in the instruction has been rewritten with the new data pattern specified in the instruction and the part is ready for another instruction. The register to be written into is not necessary to be erased before write operation. DI must be brought low during the self-timed programming cycle and status check. PE must be kept high during entering instruction.

Write-All

The write-all (WRAL) command writes all registers with the new data pattern specified in the instruction. This command is provided for device evaluation purposes only and is not meant to be used for normal operation. PE must be kept high during entering instruction.

■Instruction Set For 93C57

Instruction	Start Bit	Op-code	Address	Data	Comments
READ	01	10	A_6-A_0		READ register
WRITE	01	01	A_6-A_0	D_{15}-D_0	WRITE register
EWEN	01	00	11XXXXX		ERASE/WRITE enable
EWDS	01	00	00XXXXX		ERASE/WRITE disable
WRAL	01	00	01XXXXX	D_{15}-D_0	Write all registers

AK93C57 has 5 instructions as shown. Note that the Most Significant Bit of any given instruction is a "01" and is viewed as a start bit in the interface sequence. The next 9 bits carry the op-code and the 7-bit address for 1 of 128, 16-bit registers.

ABSOLUTE MAXIMUM RATINGS

Voltage relative to ground	−0.6V to +6.0V	Lead temperature (soldering 10 sec.)	+260°C
Ambient storage temperature	−65°C to +125°C		

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Temperature Range	0°C to +70°C	Vcc Power Supply	2.5V ~ 5.5V

NON-VOLATILE CHARACTERISTICS

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNITS
T_{DR}	Data Retention Time	Ta=70°C	10			Year
$N_{E/W}$	Write/Erase Cycles			10^4		Cycle

D.C. ELECTRICAL CHARACTERISTICS

4.5V ≦ Vcc ≦ 5.5V, 0°C ≦ Ta ≦ 70°C

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
I_{cc}	Operating Current TTL/CMOS Inputs	DO=OPEN, CS=PE=V_{IH} Vcc=5.5V, f=2MHz		5	mA
I_{ccSB1}	Standby Current TTL Inputs	Vcc=5.5V, CS=V_{IL} DO=OPEN		1	mA
I_{ccSB2}	Standby Current CMOS Inputs	Vcc=5.5V, CS=V_{IL} Inputs=V_{CC} or GND DO=OPEN		100	μA
V_{IL}	Input Voltage Low		-0.1	0.8	V
V_{IH}	Input Voltage High		2.0	Vcc+1	V
V_{OL}	Output Voltage Low	I_{OL}=2.1mA		0.4	V
V_{OH}	Output Voltage High	I_{OH}=0.4mA	2.2		V
I_{LI}	Input Leakage Current	V_{IN}=5.5V		I 10 I	μA
I_{LO}	Output Leakage Current	V_{OUT}=5.5V, CS=0V		I 10 I	μA

AK93C57 is TTL compatible under Vcc=4.5 ~ 5.5V.

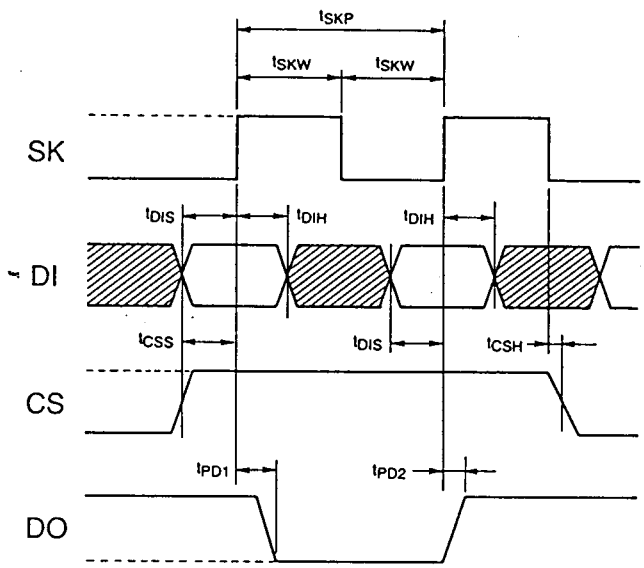
A.C. ELECTRICAL CHARACTERISTICS

4.5V ≦ Vcc ≦ 5.5V, 0°C ≦ Ta ≦ 70°C

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
t_{SKP}	SK Cycle Time		500		ns
t_{SKW}	SK Pulse Width low/high		200		ns
t_{CSS}	CS Setup Time		100		ns
t_{CSH}	CS Hold Time		0		ns
t_{DIS}	Data Setup Time		200		ns
t_{DIH}	Data Hold Time		200		ns
t_{PD1}	SK to DO Delay 1	C_L=100pF, V_{OL}=1.8V, V_{OH}=2.0V V_{IL}=0.45V, V_{IH}=2.4V		500	ns
t_{PD2}	SK to DO Delay 2			500	ns
$t_{E/W}$	Selftimed Program Cycle			10	ms
t_{CS}	Min CS Low Time		250		ns
t_{SV}	CS to Status Valid	C_L=100pF		500	ns
t_{OH}/t_{IH}	CS to Output High-Z			100	ns

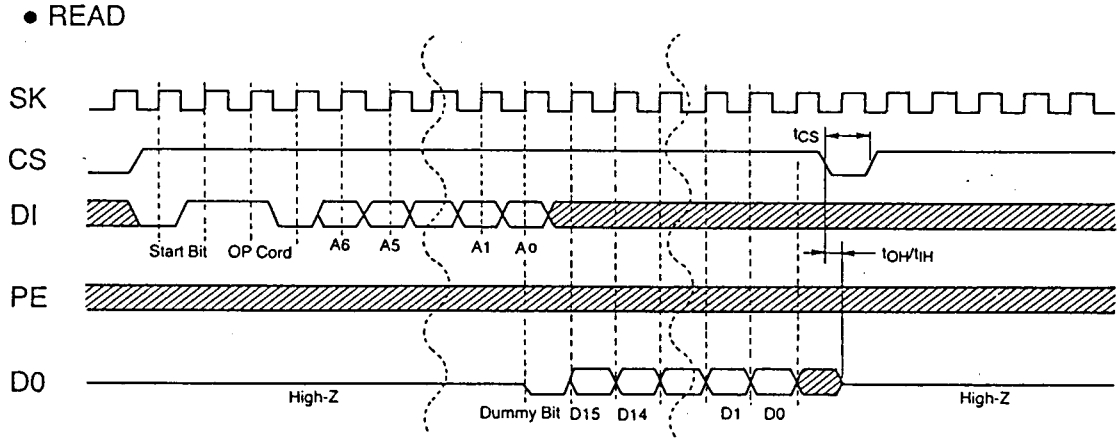
AC WAVEFORM

□Synchronous Data timing



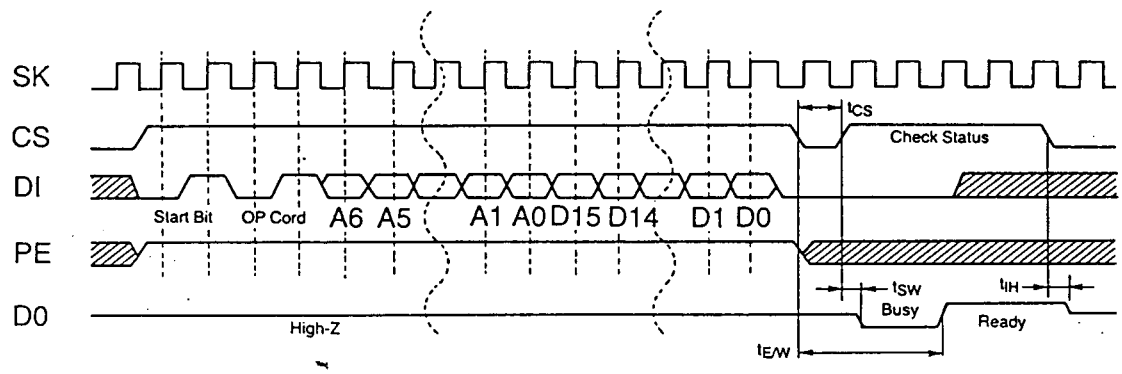
□Instruction Timing

• READ

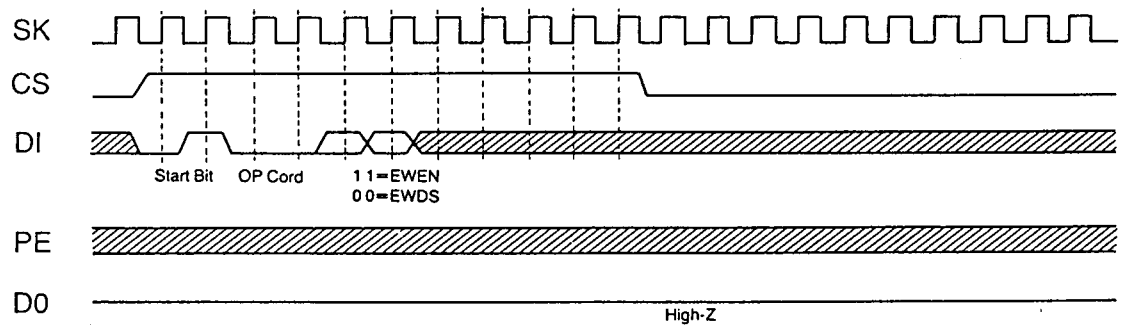


□Instruction Timing (Continued)

• WRITE



• EWEN/EWDS



• WRAL