

2SK3948G

Silicon N-channel junction FET

For impedance conversion in low frequency

For electret capacitor microphone

■ Features

- Low noise voltage NV
- High voltage gain GV
- Thin package: TSSSMini3-F2 (1.2 mm × 1.2 mm × 0.33 mm)

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain-source voltage (Gate open)	V_{DSO}	20	V
Drain-gate voltage (Source open)	V_{DGO}	20	V
Drain-source current (Gate open)	I_{DSO}	2	mA
Drain-gate current (Source open)	I_{DGO}	2	mA
Power dissipation	P_D	100	mW
Operating ambient temperature	T_{opr}	-20 to +80	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +125	$^\circ\text{C}$

■ Package

- Code
TSSSMini3-F2
- Pin Name
1: Drain
2: Source
3: Gate

■ Marking Symbol: 4X

■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain current *1	I_D	$V_{DD} = 2.0\text{ V}$, $R_d = 2.2\text{ k}\Omega \pm 1\%$	170		470	μA
Drain-source current *2	I_{DSS}	$V_{DD} = 2.0\text{ V}$, $R_d = 2.2\text{ k}\Omega \pm 1\%$, $V_{GS} = 0$	180		450	μA
Mutual conductance	g_m	$V_{DS} = 2.0\text{ V}$, $V_{GS} = 0$, $f = 1\text{ kHz}$	660	1 500		μS
Noise voltage *3	NV	$V_{DD} = 2.0\text{ V}$, $R_d = 2.2\text{ k}\Omega \pm 1\%$ $C_O = 5\text{ pF}$, A-curve			8	μV
Voltage gain	G_{V1}	$V_{DD} = 2.0\text{ V}$, $R_d = 2.2\text{ k}\Omega \pm 1\%$ $C_O = 5\text{ pF}$, $e_G = 10\text{ mV}$, $f = 1\text{ kHz}$	-5.0	-1.0		dB
	G_{V2}	$V_{DD} = 12\text{ V}$, $R_d = 2.2\text{ k}\Omega \pm 1\%$ $C_O = 5\text{ pF}$, $e_G = 10\text{ mV}$, $f = 1\text{ kHz}$	-3.0	3.0		
	G_{V3}	$V_{DD} = 1.5\text{ V}$, $R_d = 2.2\text{ k}\Omega \pm 1\%$ $C_O = 5\text{ pF}$, $e_G = 10\text{ mV}$, $f = 1\text{ kHz}$	-7.0	-1.5		
Voltage gain difference	$\Delta G_V \cdot f $ *4	$V_{DD} = 2.0\text{ V}$, $R_d = 2.2\text{ k}\Omega \pm 1\%$ $C_O = 5\text{ pF}$, $e_G = 10\text{ mV}$ $f = 1\text{ kHz to } 70\text{ Hz}$		0.0	1.7	
	$ G_{V1} - G_{V3} $			0.5	1.0	dB

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. A protection diode is built-in between gate and source of transistor. However if forward current flows between gate and source transistor might be damaged. So please be careful not insert reverse.

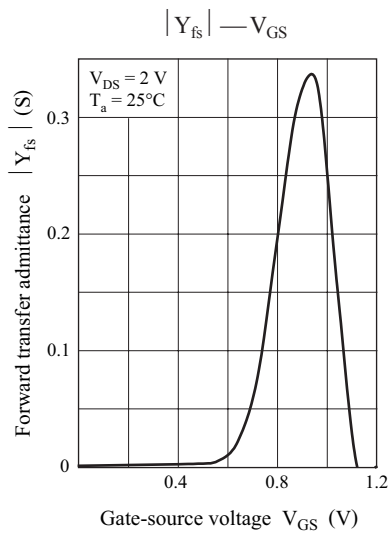
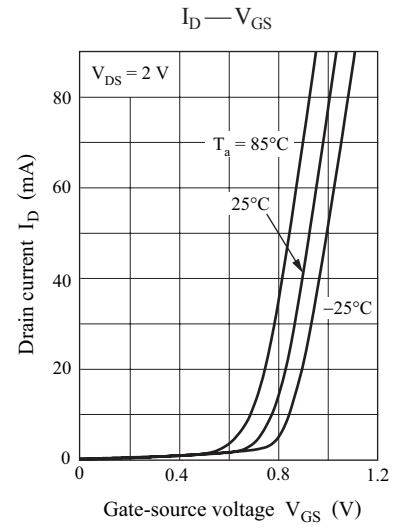
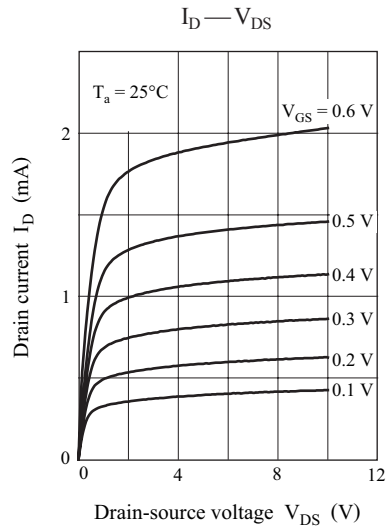
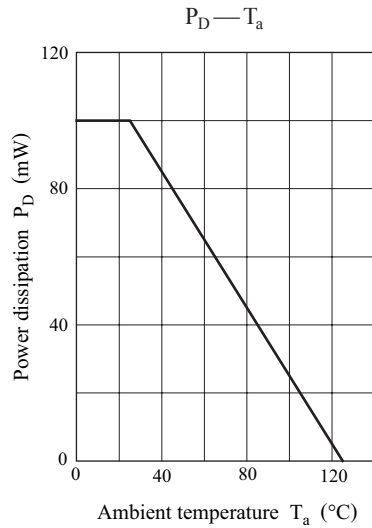
3. *1: I_D is assured for I_{DSS} .

*2: Rank classification

Rank	T	U
I_D (μA)	170 to 330	270 to 470
I_{DSS} (μA)	180 to 320	280 to 450

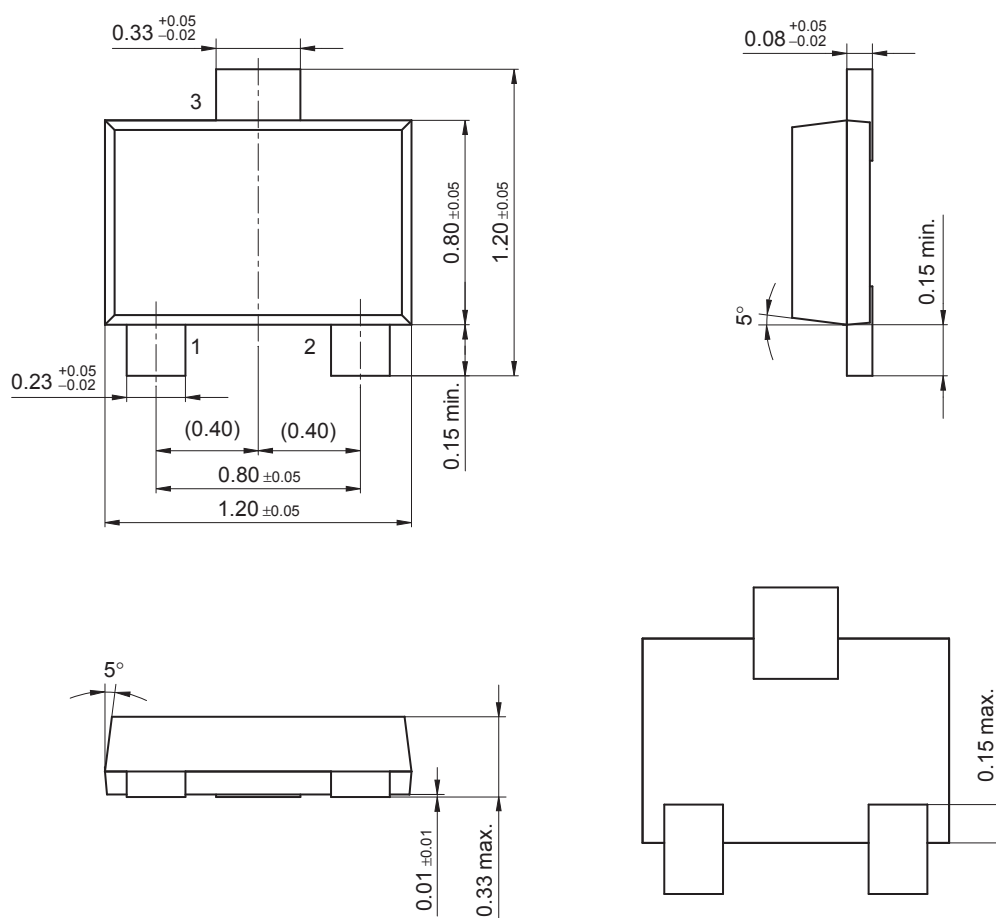
*3: NV is assured for design.

*4: $\Delta |G_V \cdot f|$ is assured for AQL 0.065. (The measurement method is used by source-grounded circuit.)



TSSSMini3-F2

Unit: mm



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