TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOSIII)

# SSM6K24FE

#### **High Speed Switching Applications**

• Optimum for high-density mounting in small packages

• Low on-resistance:  $R_{on} = 145m\Omega \text{ (max) } (@V_{GS} = 4.5 \text{ V})$ 

 $R_{on} = 180 m\Omega \text{ (max) (@V_{GS} = 2.5 V)}$ 

### Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		$V_{DS}$	30	V	
Gate-Source voltage		V <sub>GSS</sub>	± 12	V	
Drain current	DC	I <sub>D</sub>	0.5	Α	
	Pulse	I <sub>DP</sub>	1.5	A	
Drain power dissipation		P <sub>D</sub> (Note 1)	500	mW	
Channel temperature		T <sub>ch</sub>	150	°C	
Storage temperature range		T <sub>stg</sub>	-55~150	°C	

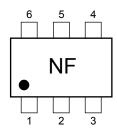
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the

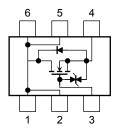
Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board. (25.4 mm  $\times$  25.4 mm  $\times$  1.6 t, Cu Pad: 645 mm  $^2$  )

# Marking



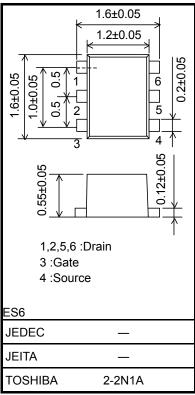
# **Equivalent Circuit (top view)**



## **Handling Precaution**

When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Unit: mm



Weight: 3.0 mg (typ.)

### **Electrical Characteristics (Ta = 25°C)**

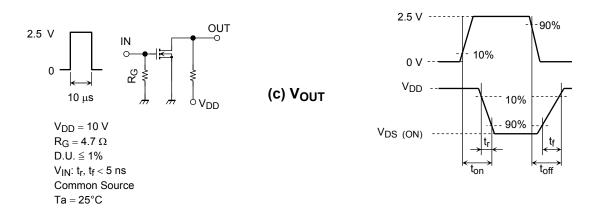
Chara	cteristics	Symbol	Test Condition	Min	Тур.	Max	Unit	
Gate leakage curr	ent	I <sub>GSS</sub>	$V_{GS} = \pm 12 \text{ V}, V_{DS} = 0$	_	_	±1	μА	
Drain-Source breakdown voltage		V (BR) DSS	$I_D = 1$ mA, $V_{GS} = 0$	30	_	_	- V	
		V (BR) DSX	$I_D = 1 \text{ mA}, V_{GS} = -12 \text{ V}$	18	_	_		
Drain cut-off curre	ent	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0	_	_	1	μА	
Gate threshold voltage		V <sub>th</sub>	V <sub>DS</sub> = 3 V, I <sub>D</sub> = 0.1 mA	0.5	_	1.1	V	
Forward transfer admittance		Y <sub>fs</sub>	$V_{DS} = 3 \text{ V}, I_D = 0.25 \text{ A}$ (Note2)	1.0	2.0	_	S	
Drain-Source on-resistance		R <sub>DS (ON)</sub>	$I_D = 0.50 \text{ A}, V_{GS} = 4.5 \text{ V}$ (Note2)	_	120	145	- mΩ	
			I <sub>D</sub> = 0.25 A, V <sub>GS</sub> = 2.5 V (Note2)	_	140	180		
Input capacitance		C <sub>iss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0, f = 1 MHz	_	245	_	pF	
Reverse transfer capacitance		C <sub>rss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0, f = 1 MHz	_	33	_	pF	
Output capacitance		Coss	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0, f = 1 MHz	_	41	_	pF	
Switching time	Turn-on time	t <sub>on</sub>	V <sub>DD</sub> = 10 V, I <sub>D</sub> = 0.25 A,	_	9	_	- ns	
	Turn-off time	t <sub>off</sub>	$V_{GS} = 0 \sim 2.5 \text{ V}, R_G = 4.7 \Omega$	_	15	_		

Note2: Pulse test

# **Switching Time Test Circuit**





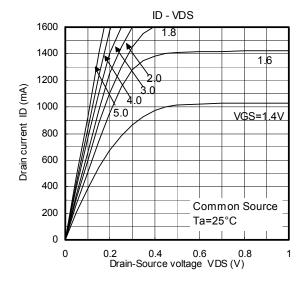


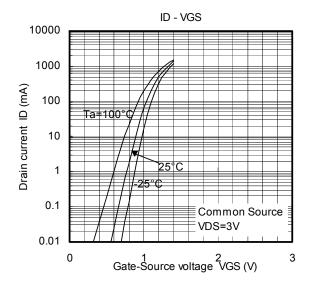
#### **Precaution**

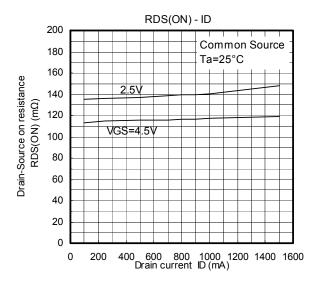
 $V_{th}$  can be expressed as the voltage between gate and source when the low operating current value is  $I_D$  = 100  $\mu$ A for this product. For normal switching operation,  $V_{GS~(on)}$  requires a higher voltage than  $V_{th}$  and  $V_{GS~(off)}$  requires a lower voltage than  $V_{th}$ .

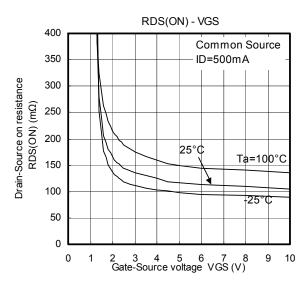
(The relationship can be established as follows:  $V_{GS (off)} < V_{th} < V_{GS (on)}$ )

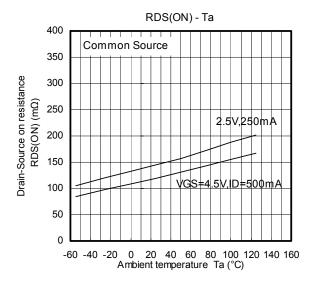
Please take this into consideration when using the device.

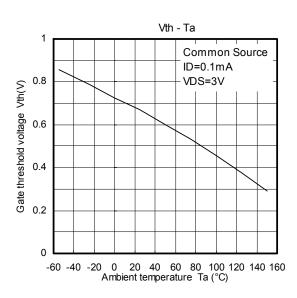


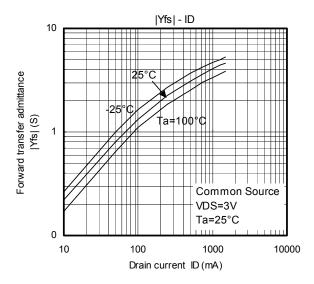


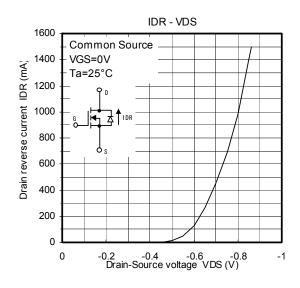


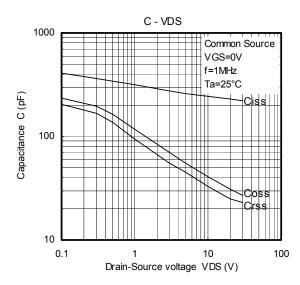


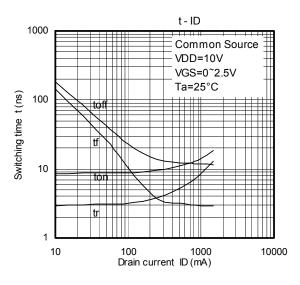


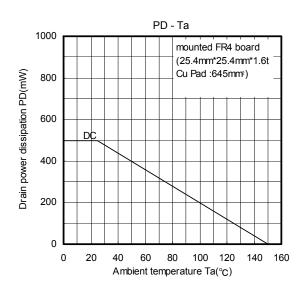












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