

# DATA SHEET

## **74AHC1G00; 74AHCT1G00** 2-input NAND gate

Product specification  
Supersedes data of 2002 Feb 27

2002 May 27

## 2-input NAND gate

## 74AHC1G00; 74AHCT1G00

## FEATURES

- Symmetrical output impedance
- High noise immunity
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - CDM EIA/JESD22-C101 exceeds 1000 V.
- Low power dissipation
- Balanced propagation delays
- Very small 5-pin package
- Output capability: standard
- Specified from –40 to +125 °C.

## DESCRIPTION

The 74AHC1G/AHCT1G00 is a high-speed Si-gate CMOS device.

The 74AHC1G/AHCT1G00 provides the 2-input NAND function.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ °C}$ ;  $t_r = t_f \leq 3.0\text{ ns}$ .

| SYMBOL            | PARAMETER                      | CONDITIONS  | TYPICAL |        | UNIT |
|-------------------|--------------------------------|---|---------|--------|------|
|                   |                                |   | AHC1G   | AHCT1G |      |
| $t_{PHL}/t_{PLH}$ | propagation delay A and B to Y | $C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$              | 3.5     | 3.6    | ns   |
| $C_I$             | input capacitance              |   | 1.5     | 1.5    | pF   |
| $C_{PD}$          | power dissipation capacitance  | $C_L = 50\text{ pF}$ ; $f = 1\text{ MHz}$ ; notes 1 and 2 | 17      | 18     | pF   |

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in Volts.

2. The condition is  $V_i = \text{GND to } V_{CC}$ .

## 2-input NAND gate

## 74AHC1G00; 74AHCT1G00

## FUNCTION TABLE

See note 1.

| INPUTS |   | OUTPUT |
|--------|---|--------|
| A      | B | Y      |
| L      | L | H      |
| L      | H | H      |
| H      | L | H      |
| H      | H | L      |

## Note

1. H = HIGH voltage level;  
L = LOW voltage level.

## ORDERING INFORMATION

| TYPE NUMBER  | PACKAGES          |      |         |          |        |         |
|--------------|-------------------|------|---------|----------|--------|---------|
|              | TEMPERATURE RANGE | PINS | PACKAGE | MATERIAL | CODE   | MARKING |
| 74AHC1G00GW  | -40 to +125 °C    | 5    | SC-88A  | plastic  | SOT353 | AA      |
| 74AHCT1G00GW | -40 to +125 °C    | 5    | SC-88A  | plastic  | SOT353 | CA      |
| 74AHC1G00GV  | -40 to +125 °C    | 5    | SC-74A  | plastic  | SOT753 | A00     |
| 74AHCT1G00GV | -40 to +125 °C    | 5    | SC-74A  | plastic  | SOT753 | C00     |

## PINNING

| PIN | SYMBOL          | DESCRIPTION    |
|-----|-----------------|----------------|
| 1   | B               | data input B   |
| 2   | A               | data input A   |
| 3   | GND             | ground (0 V)   |
| 4   | Y               | data output Y  |
| 5   | V <sub>CC</sub> | supply voltage |

# 2-input NAND gate

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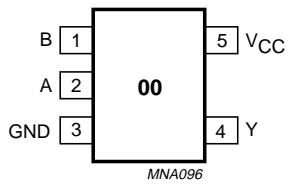


Fig.1 Pin configuration.

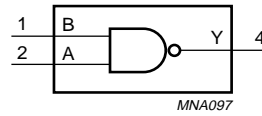


Fig.2 Logic symbol.



Fig.3 IEC logic symbol.

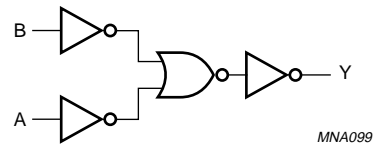


Fig.4 Logic diagram.

## 2-input NAND gate

## 74AHC1G00; 74AHCT1G00

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL                                | PARAMETER                     | CONDITIONS                               | 74AHC1G |      |          | 74AHCT1G |      |          | UNIT |
|---------------------------------------|-------------------------------|--|---------|------|----------|----------|------|----------|------|
|                                       |                               |  | MIN.    | TYP. | MAX.     | MIN.     | TYP. | MAX.     |      |
| $V_{CC}$                              | supply voltage                |  | 2.0     | 5.0  | 5.5      | 4.5      | 5.0  | 5.5      | V    |
| $V_I$                                 | input voltage                 |  | 0       | –    | 5.5      | 0        | –    | 5.5      | V    |
| $V_O$                                 | output voltage                |  | 0       | –    | $V_{CC}$ | 0        | –    | $V_{CC}$ | V    |
| $T_{amb}$                             | operating ambient temperature | see DC and AC characteristics per device | –40     | +25  | +125     | –40      | +25  | +125     | °C   |
| $t_r, t_f$<br>( $\Delta t/\Delta f$ ) | input rise and fall times     | $V_{CC} = 3.3 \pm 0.3$ V                 | –       | –    | 100      | –        | –    | –        | ns/V |
|                                       |                               | $V_{CC} = 5 \pm 0.5$ V                   | –       | –    | 20       | –        | –    | 20       | ns/V |

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

| SYMBOL    | PARAMETER                     | CONDITIONS                                       | MIN. | MAX.     | UNIT |
|-----------|-------------------------------|--|------|----------|------|
| $V_{CC}$  | supply voltage                |  | –0.5 | +7.0     | V    |
| $V_I$     | input voltage                 |  | –0.5 | +7.0     | V    |
| $I_{IK}$  | input diode current           | $V_I < -0.5$ V                                   | –    | –20      | mA   |
| $I_{OK}$  | output diode current          | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V; note 1 | –    | $\pm 20$ | mA   |
| $I_O$     | output source or sink current | $-0.5$ V $< V_O < V_{CC} + 0.5$ V                | –    | $\pm 25$ | mA   |
| $I_{CC}$  | $V_{CC}$ or GND current       |  | –    | $\pm 75$ | mA   |
| $T_{stg}$ | storage temperature           |  | –65  | +150     | °C   |
| $P_D$     | power dissipation per package | for temperature range from –40 to +125 °C        | –    | 250      | mW   |

## Note

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 2-input NAND gate

## 74AHC1G00; 74AHCT1G00

## DC CHARACTERISTICS

## Family 74AHC1G

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| SYMBOL          | PARAMETER                 | TEST CONDITIONS   | T <sub>amb</sub> (°C) |                        |      |      |      |            |      |             | UNIT |      |
|-----------------|---------------------------|---|-----------------------|------------------------|------|------|------|------------|------|-------------|------|------|
|                 |                           |   | OTHER                 | V <sub>CC</sub><br>(V) | 25   |      |      | -40 to +85 |      | -40 to +125 |      |      |
|                 |                           |   |                       |                        | MIN. | TYP. | MAX. | MIN.       | MAX. | MIN.        |      | MAX. |
| V <sub>IH</sub> | HIGH-level input voltage  |   | 2.0                   | 1.5                    | –    | –    | 1.5  | –          | 1.5  | –           | V    |      |
|                 |                           |   | 3.0                   | 2.1                    | –    | –    | 2.1  | –          | 2.1  | –           | V    |      |
|                 |                           |   | 5.5                   | 3.85                   | –    | –    | 3.85 | –          | 3.85 | –           | V    |      |
| V <sub>IL</sub> | LOW-level input voltage   |   | 2.0                   | –                      | –    | 0.5  | –    | 0.5        | –    | 0.5         | V    |      |
|                 |                           |   | 3.0                   | –                      | –    | 0.9  | –    | 0.9        | –    | 0.9         | V    |      |
|                 |                           |   | 5.5                   | –                      | –    | 1.65 | –    | 1.65       | –    | 1.65        | V    |      |
| V <sub>OH</sub> | HIGH-level output voltage | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>I <sub>O</sub> = –50 µA  | 2.0                   | 1.9                    | 2.0  | –    | 1.9  | –          | 1.9  | –           | V    |      |
|                 |                           | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>I <sub>O</sub> = –50 µA  | 3.0                   | 2.9                    | 3.0  | –    | 2.9  | –          | 2.9  | –           | V    |      |
|                 |                           | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>I <sub>O</sub> = –50 µA  | 4.5                   | 4.4                    | 4.5  | –    | 4.4  | –          | 4.4  | –           | V    |      |
|                 |                           | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>I <sub>O</sub> = –4.0 mA | 3.0                   | 2.58                   | –    | –    | 2.48 | –          | 2.40 | –           | V    |      |
|                 |                           | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>I <sub>O</sub> = –8.0 mA | 4.5                   | 3.94                   | –    | –    | 3.8  | –          | 3.70 | –           | V    |      |
| V <sub>OL</sub> | LOW-level output voltage  | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>I <sub>O</sub> = 50 µA   | 2.0                   | –                      | 0    | 0.1  | –    | 0.1        | –    | 0.1         | V    |      |
|                 |                           | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>I <sub>O</sub> = 50 µA   | 3.0                   | –                      | 0    | 0.1  | –    | 0.1        | –    | 0.1         | V    |      |
|                 |                           | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>I <sub>O</sub> = 50 µA   | 4.5                   | –                      | 0    | 0.1  | –    | 0.1        | –    | 0.1         | V    |      |
|                 |                           | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>I <sub>O</sub> = 4.0 mA  | 3.0                   | –                      | –    | 0.36 | –    | 0.44       | –    | 0.55        | V    |      |
|                 |                           | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>I <sub>O</sub> = 8.0 mA  | 4.5                   | –                      | –    | 0.36 | –    | 0.44       | –    | 0.55        | V    |      |
| I <sub>LI</sub> | input leakage current     | V <sub>I</sub> = V <sub>CC</sub> or GND   | 5.5                   | –                      | –    | 0.1  | –    | 1.0        | –    | 2.0         | µA   |      |
| I <sub>CC</sub> | quiescent supply current  | V <sub>I</sub> = V <sub>CC</sub> or GND;<br>I <sub>O</sub> = 0                    | 5.5                   | –                      | –    | 1.0  | –    | 10         | –    | 40          | µA   |      |
| C <sub>I</sub>  | input capacitance         |   |                       | –                      | 1.5  | 10   | –    | 10         | –    | 10          | pF   |      |

## 2-input NAND gate

## 74AHC1G00; 74AHCT1G00

**Family 74AHCT1G**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| SYMBOL           | PARAMETER   | TEST CONDITIONS  |                     | T <sub>amb</sub> (°C) |      |      |            |      |             | UNIT |      |
|------------------|---|--|---------------------|-----------------------|------|------|------------|------|-------------|------|------|
|                  |   | OTHER  | V <sub>CC</sub> (V) | 25                    |      |      | -40 to +85 |      | -40 to +125 |      |      |
|                  |   |  |                     | MIN.                  | TYP. | MAX. | MIN.       | MAX. | MIN.        |      | MAX. |
| V <sub>IH</sub>  | HIGH-level input voltage                          |  | 4.5 to 5.5          | 2.0                   | –    | –    | 2.0        | –    | 2.0         | –    | V    |
| V <sub>IL</sub>  | LOW-level input voltage                           |  | 4.5 to 5.5          | –                     | –    | 0.8  | –          | 0.8  | –           | 0.8  | V    |
| V <sub>OH</sub>  | HIGH-level output voltage                         | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>I <sub>O</sub> = –50 µA         | 4.5                 | 4.4                   | 4.5  | –    | 4.4        | –    | 4.4         | –    | V    |
|                  |   | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>I <sub>O</sub> = –8.0 mA        | 4.5                 | 3.94                  | –    | –    | 3.8        | –    | 3.70        | –    | V    |
| V <sub>OL</sub>  | LOW-level output voltage                          | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>I <sub>O</sub> = 50 µA          | 4.5                 | –                     | 0    | 0.1  | –          | 0.1  | –           | 0.1  | V    |
|                  |   | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>I <sub>O</sub> = 8.0 mA         | 4.5                 | –                     | –    | 0.36 | –          | 0.44 | –           | 0.55 | V    |
| I <sub>LI</sub>  | input leakage current                             | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>                                      | 5.5                 | –                     | –    | 0.1  | –          | 1.0  | –           | 2.0  | µA   |
| I <sub>CC</sub>  | quiescent supply current                          | V <sub>I</sub> = V <sub>CC</sub> or GND;<br>I <sub>O</sub> = 0                           | 5.5                 | –                     | –    | 1.0  | –          | 10   | –           | 40   | µA   |
| ΔI <sub>CC</sub> | additional quiescent supply current per input pin | V <sub>I</sub> = 3.4 V;<br>other inputs at V <sub>CC</sub> or GND;<br>I <sub>O</sub> = 0 | 5.5                 | –                     | –    | 1.35 | –          | 1.5  | –           | 1.5  | mA   |
| C <sub>I</sub>   | input capacitance                                 |  |                     | –                     | 1.5  | 10   | –          | 10   | –           | 10   | pF   |

## 2-input NAND gate

## 74AHC1G00; 74AHCT1G00

## AC CHARACTERISTICS

## Type 74AHC1G00

GND = 0 V;  $t_r = t_f \leq 3.0$  ns.

| SYMBOL                                       | PARAMETER                         | TEST CONDITIONS  |                        | T <sub>amb</sub> (°C) |      |      |            |      |             | UNIT |      |
|--|-----------------------------------|------------------|------------------------|-----------------------|------|------|------------|------|-------------|------|------|
|  |                                   | WAVEFORMS        | C <sub>L</sub><br>(pF) | 25                    |      |      | -40 to +85 |      | -40 to +125 |      |      |
|  |                                   |                  |                        | MIN.                  | TYP. | MAX. | MIN.       | MAX. | MIN.        |      | MAX. |
| <b>V<sub>CC</sub> = 3.0 to 3.6 V; note 1</b> |                                   |                  |                        |                       |      |      |            |      |             |      |      |
| t <sub>PHL</sub> /t <sub>PLH</sub>           | propagation delay<br>A and B to Y | see Figs 5 and 6 | 15                     | –                     | 4.5  | 7.9  | 1.0        | 9.5  | 1.0         | 10.5 | ns   |
|  |                                   |                  | 50                     | –                     | 6.5  | 11.4 | 1.0        | 13.0 | 1.0         | 14.5 | ns   |
| <b>V<sub>CC</sub> = 4.5 to 5.5 V; note 2</b> |                                   |                  |                        |                       |      |      |            |      |             |      |      |
| t <sub>PHL</sub> /t <sub>PLH</sub>           | propagation delay<br>A and B to Y | see Figs 5 and 6 | 15                     | –                     | 3.5  | 5.5  | 1.0        | 6.5  | 1.0         | 7.0  | ns   |
|  |                                   |                  | 50                     | –                     | 4.9  | 7.5  | 1.0        | 8.5  | 1.0         | 9.5  | ns   |

## Notes

1. Typical values at V<sub>CC</sub> = 3.3 V.
2. Typical values at V<sub>CC</sub> = 5 V.

## Type 74AHCT1G00

GND = 0 V;  $t_r = t_f \leq 3.0$  ns.

| SYMBOL                                       | PARAMETER                         | TEST CONDITIONS  |                        | T <sub>amb</sub> (°C) |      |      |            |      |             | UNIT |      |
|--|-----------------------------------|------------------|------------------------|-----------------------|------|------|------------|------|-------------|------|------|
|  |                                   | WAVEFORMS        | C <sub>L</sub><br>(pF) | 25                    |      |      | -40 to +85 |      | -40 to +125 |      |      |
|  |                                   |                  |                        | MIN.                  | TYP. | MAX. | MIN.       | MAX. | MIN.        |      | MAX. |
| <b>V<sub>CC</sub> = 4.5 to 5.5 V; note 1</b> |                                   |                  |                        |                       |      |      |            |      |             |      |      |
| t <sub>PHL</sub> /t <sub>PLH</sub>           | propagation delay<br>A and B to Y | see Figs 5 and 6 | 15                     | –                     | 3.6  | 6.2  | 1.0        | 7.1  | 1.0         | 8.0  | ns   |
|  |                                   |                  | 50                     | –                     | 5.0  | 7.9  | 1.0        | 9.0  | 1.0         | 10.0 | ns   |

## Note

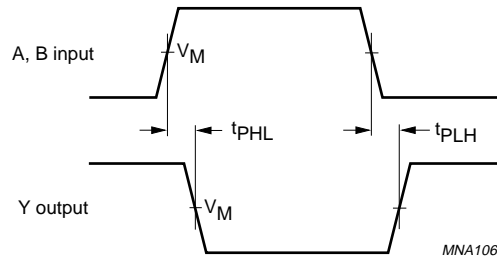
1. Typical values at V<sub>CC</sub> = 5 V.



2-input NAND gate

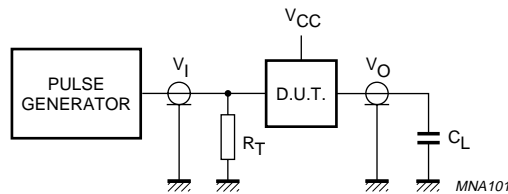
74AHC1G00; 74AHCT1G00

AC WAVEFORMS



| FAMILY | V <sub>I</sub> INPUT REQUIREMENTS | V <sub>M</sub> INPUT | V <sub>M</sub> OUTPUT |
|--------|-----------------------------------|----------------------|-----------------------|
| AHC1G  | GND to V <sub>CC</sub>            | 50% V <sub>CC</sub>  | 50% V <sub>CC</sub>   |
| AHCT1G | GND to 3.0 V                      | 1.5 V                | 50% V <sub>CC</sub>   |

Fig.5 The inputs (A and B) to output (Y) propagation delays.



Definitions for test circuit:

C<sub>L</sub> = Load capacitance including jig and probe capacitance (see Chapter "AC characteristics").

R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>0</sub> of the pulse generator.

Fig.6 Load circuitry for switching times.

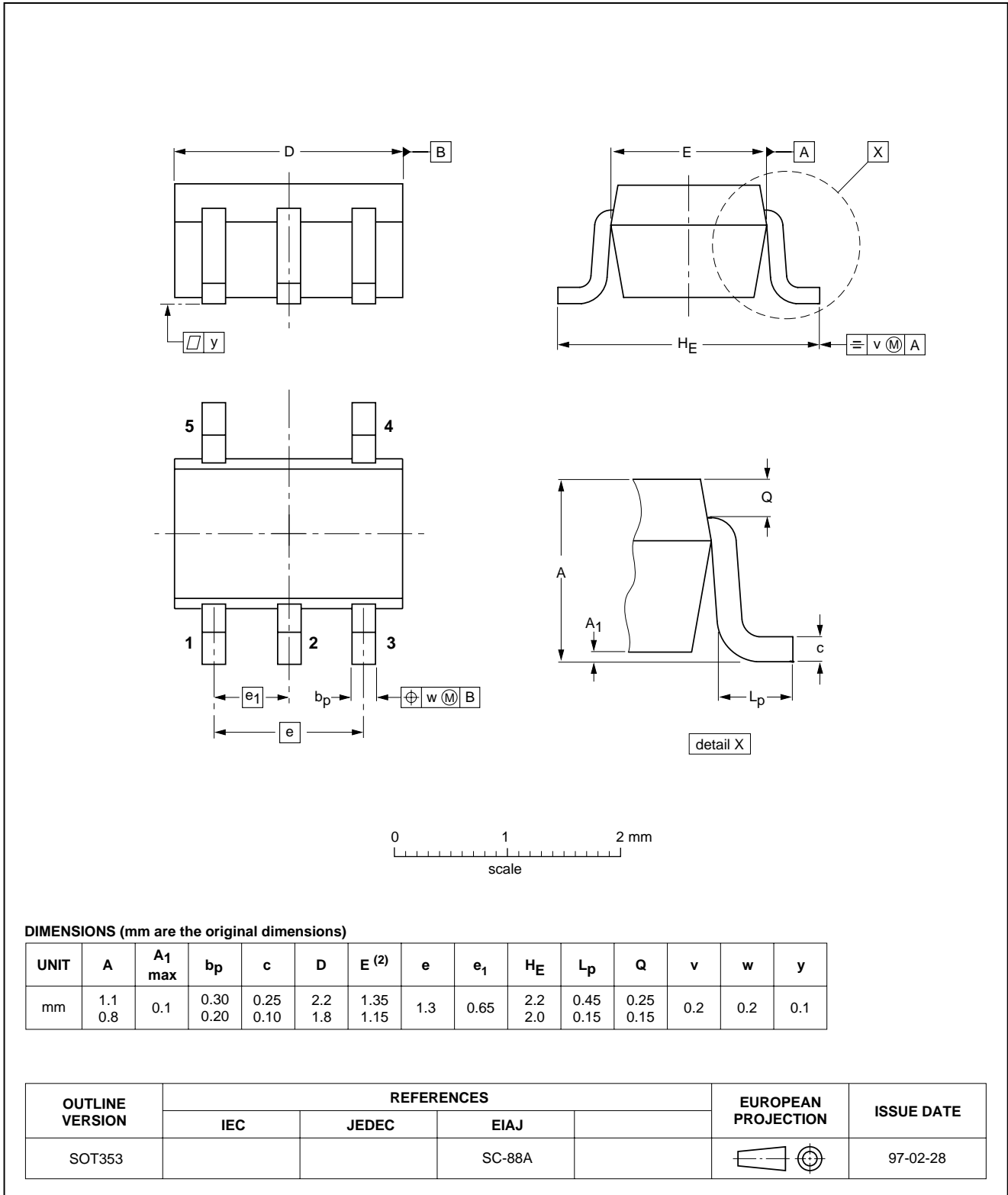
2-input NAND gate

74AHC1G00; 74AHCT1G00

PACKAGE OUTLINES

Plastic surface mounted package; 5 leads

SOT353

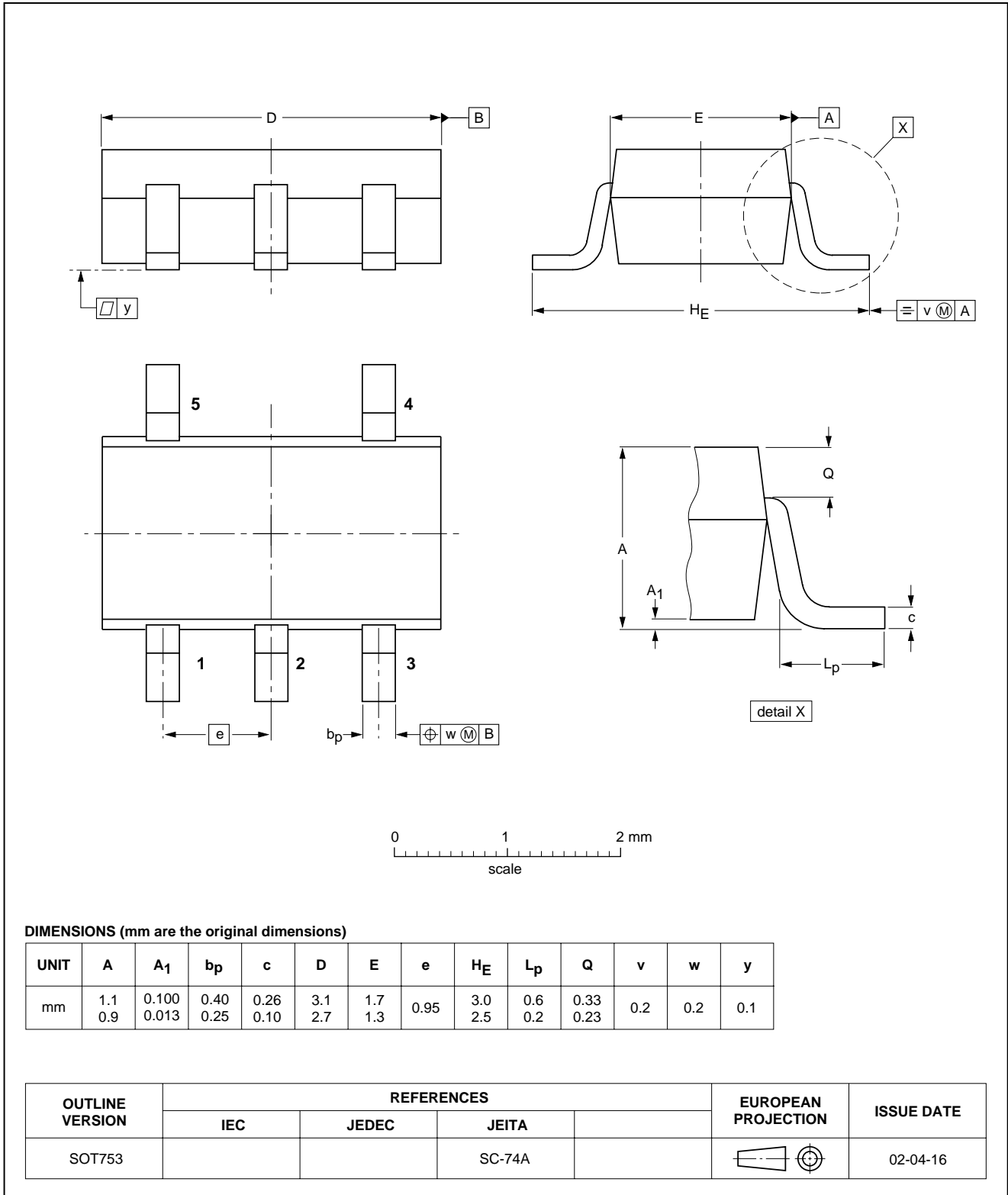


2-input NAND gate

74AHC1G00; 74AHCT1G00

Plastic surface mounted package; 5 leads

SOT753



## 2-input NAND gate

## 74AHC1G00; 74AHCT1G00

### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## 2-input NAND gate

## 74AHC1G00; 74AHCT1G00

## Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE <sup>(1)</sup>   | SOLDERING METHOD                  |                       |
|--|-----------------------------------|-----------------------|
|  | WAVE                              | REFLOW <sup>(2)</sup> |
| BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA                             | not suitable                      | suitable              |
| HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable <sup>(3)</sup>       | suitable              |
| PLCC <sup>(4)</sup> , SO, SOJ                                    | suitable                          | suitable              |
| LQFP, QFP, TQFP  | not recommended <sup>(4)(5)</sup> | suitable              |
| SSOP, TSSOP, VSO   | not recommended <sup>(6)</sup>    | suitable              |

## Notes

1. For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## 2-input NAND gate

## 74AHC1G00; 74AHCT1G00

## DATA SHEET STATUS

| DATA SHEET STATUS <sup>(1)</sup> | PRODUCT STATUS <sup>(2)</sup> | DEFINITIONS  |
|----------------------------------|-------------------------------|--|
| Objective data                   | Development                   | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.  |
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## Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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2-input NAND gate

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**NOTES**

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