TOSHIBA FIELD EFFECT TRANSISTOR SILICON N CHANNEL MOS TYPE

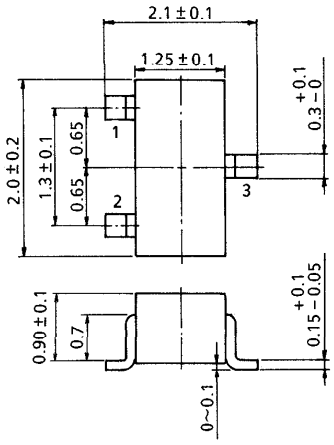
2SK1829

HIGH SPEED SWITCHING APPLICATIONS

ANALOG SWITCH APPLICATIONS

- 2.5V Gate Drive
- Low Threshold Voltage : V_{th} = 0.5~1.5V
- High Speed
- Enhanncement-Mode
- Small Package

Unit in mm

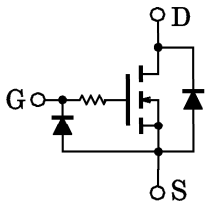


1. GATE
2. SOURCE
3. DRAIN

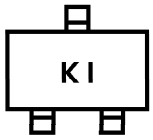
USM	
JEDEC	—
EIAJ	SC-70
TOSHIBA	2-2E1E

Weight : 0.006g (Typ.)

EQUIVALENT CIRCUIT



MARKING



This transistor is electrostatic sensitive device.
Please handle with caution.

MAXIMUM RATINGS (Ta = 25°C)

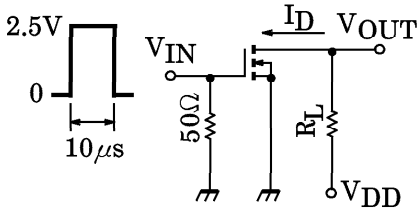
CHARACTERISTIC	SYMBOL	RATING	UNIT
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GSS}	10	V
DC Drain Current	I_D	50	mA
Drain Power Dissipation	P_D	100	mW
Channel Temperature	T_{ch}	150	°C
Storage Temperature Range	T_{stg}	−55~150	°C

000707EAA1

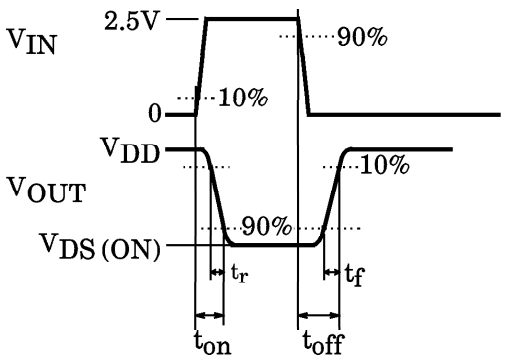
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GSS}	V_{GS} = 10V, V_{DS} = 0	—	—	1	μA
Drain-Source Breakdown Voltage		$V_{(BR)\,DSS}$	I_D = 100μA, V_{GS} = 0	20	—	—	V
Drain Cut-off Current		I_{DSS}	V_{DS} = 20V, V_{GS} = 0	—	—	1	μA
Gate Threshold Voltage		V_{th}	V_{DS} = 3V, I_D = 0.1mA	0.5	—	1.5	V
Forward Transfer Admittance		$\|Y_{fs}\|$	V_{DS} = 3V, I_D = 10mA	20	—	—	mS
Drain-Source ON Resistance		$R_{DS\,(ON)}$	I_D = 10mA, V_{GS} = 2.5V	—	20	40	Ω
Input Capacitance		C_{iss}	V_{DS} = 3V, V_{GS} = 0, f = 1MHz	—	5.5	—	pF
Reverse Transfer Capacitance		C_{rss}	V_{DS} = 3V, V_{GS} = 0, f = 1MHz	—	1.6	—	pF
Output Capacitance		C_{oss}	V_{DS} = 3V, V_{GS} = 0, f = 1MHz	—	6.5	—	pF
Switching Time	Turn-on Time	t_{on}	V_{DD} = 3V, I_D = 10mA, V_{GS} = 0~2.5V	—	0.14	—	μs
	Turn-off Time	t_{off}	V_{DD} = 3V, I_D = 10mA, V_{GS} = 0~2.5V	—	0.14	—	μs

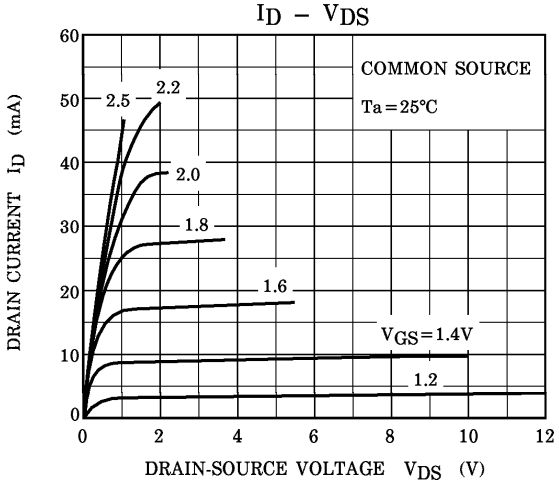
SWITCHING TIME TEST CIRCUIT



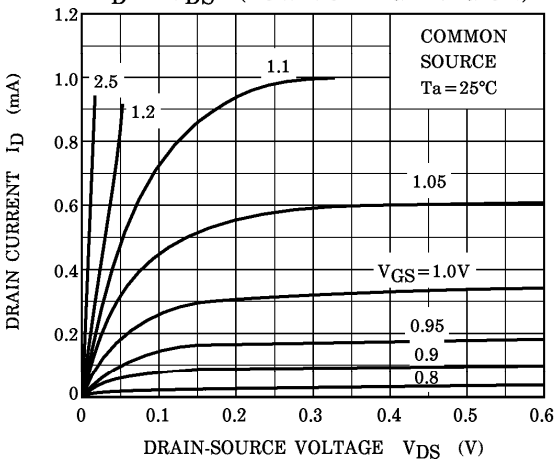
V_{DD} = 3V
D.U. ≦ 1%
V_{IN} : t_r, t_f < 5ns
(Z_{out} = 50Ω)
COMMON SOURCE
Ta = 25°C



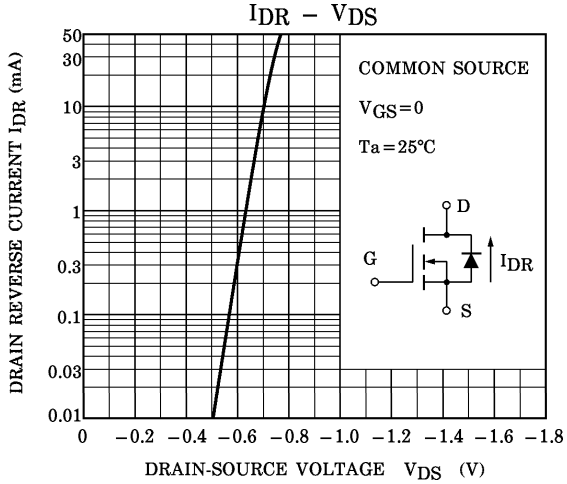
I_D – V_{DS}



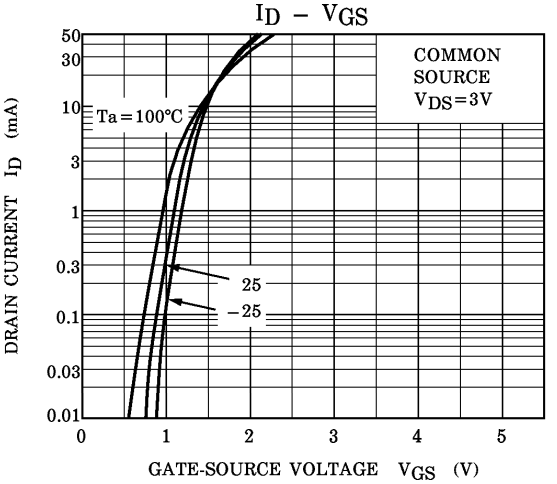
I_D – V_{DS} (LOW VOLTAGE REGION)



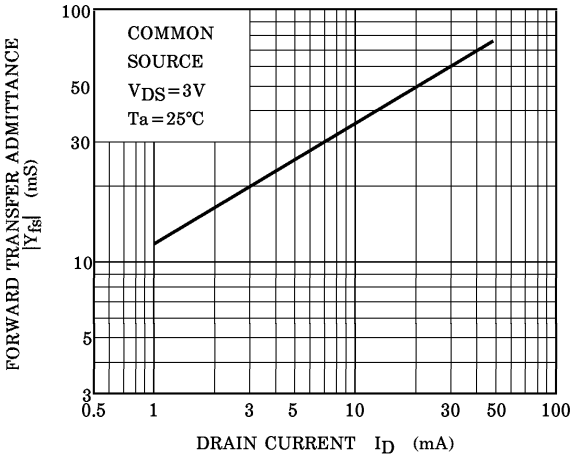
I_{DR} – V_{DS}



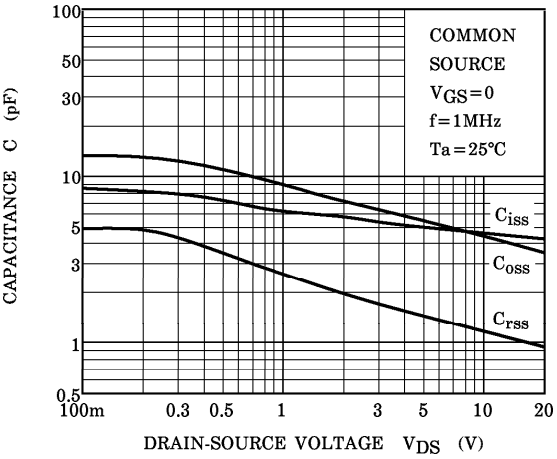
I_D – V_{GS}



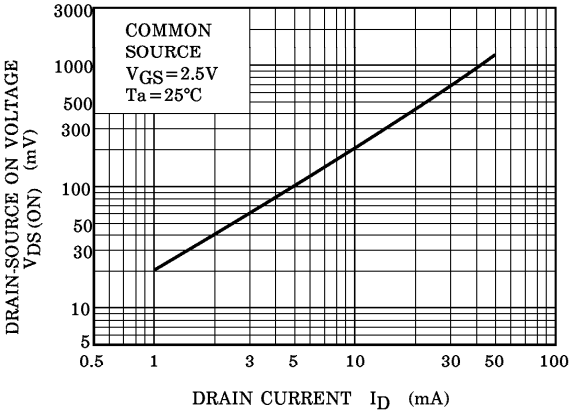
$|Y_{fs}|$ – I_D



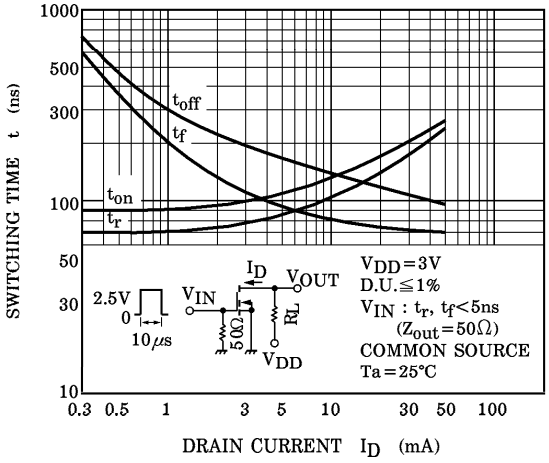
C – V_{DS}



$V_{DS\,(ON)}$ – I_D



t – I_D



P_D – Ta