

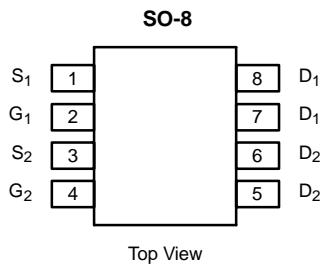


Dual P-Channel 30-V(D-S) MOSFET

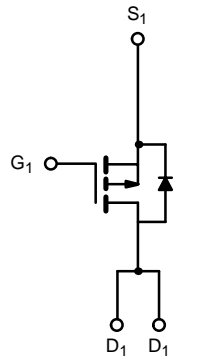
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.053 @ $V_{GS} = -10$ V	-4.9
	0.095 @ $V_{GS} = -4.5$ V	-3.6

FEATURES

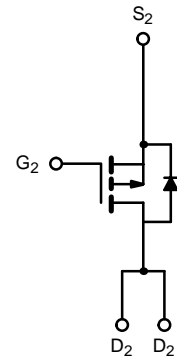
- 100% R_g Tested



Ordering Information: Si4953DY
Si4953DY-T1 (with Tape and Reel)



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	-4.9	A
	$T_A = 70^\circ\text{C}$		-3.9	
Pulsed Drain Current		I_{DM}	-30	
Continuous Source Current (Diode Conduction) ^a		I_S	-1.7	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	2.0	W
	$T_A = 70^\circ\text{C}$		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C}/\text{W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com>

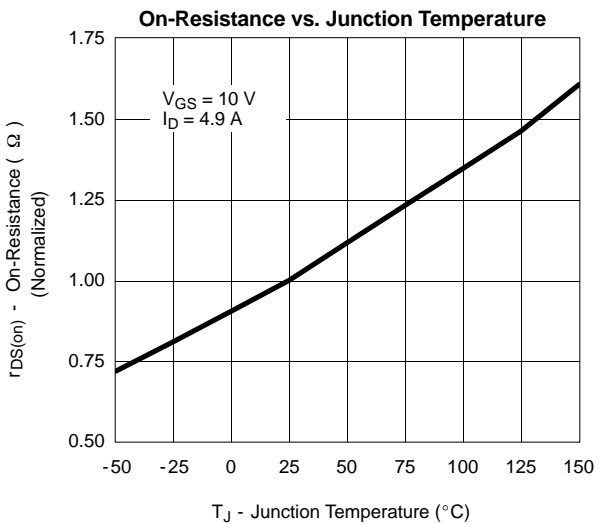
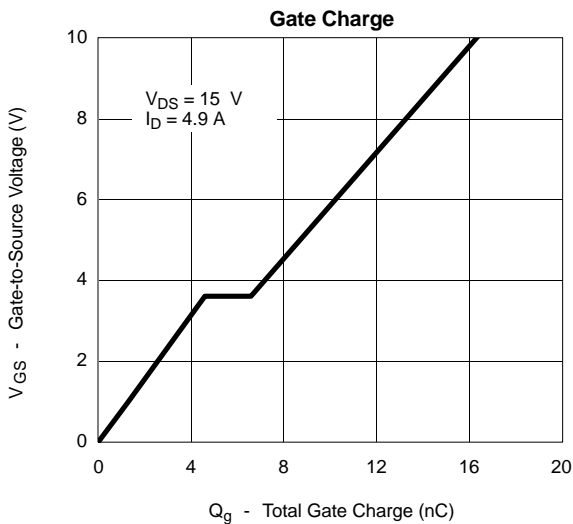
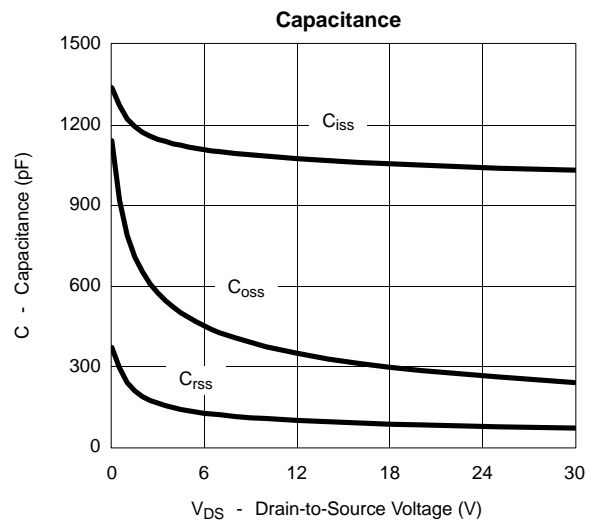
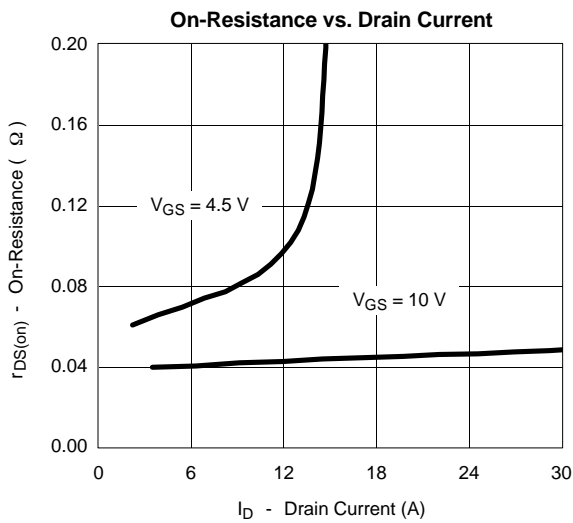
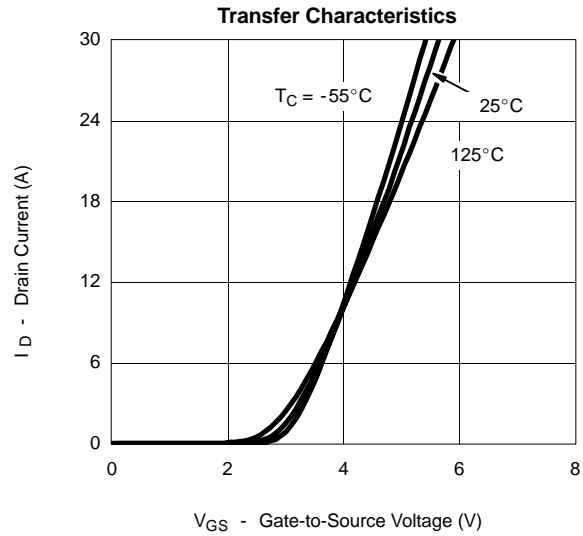
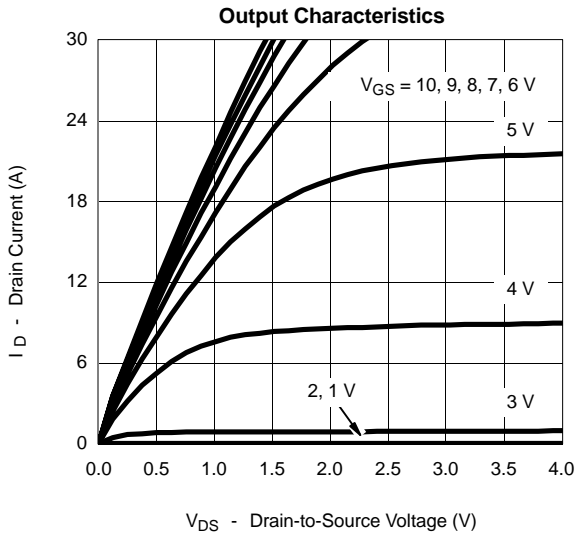
SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -30 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -30 V, V _{GS} = 0 V, T _J = 55 °C			-25	
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -10 V	-20			A
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = -10 V, I _D = -4.9 A		0.043	0.053	Ω
		V _{GS} = -4.5 V, I _D = -3.6 A		0.070	0.095	
Forward Transconductance ^b	g _{fs}	V _{DS} = -15 V, I _D = -4.9 A		10		S
Diode Forward Voltage ^b	V _{SD}	I _S = -1.7 A, V _{GS} = 0 V		0.8	-1.2	V
Dynamic^a						
Total Gate Charge	Q _g	V _{DS} = -15 V, V _{GS} = -10 V, I _D = -4.9 A		16	25	nC
Gate-Source Charge	Q _{gs}			5		
Gate-Drain Charge	Q _{gd}			2		
Gate Resistance	R _g		2		7.1	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = -15 V, R _L = 15 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _G = 6 Ω		9	15	ns
Rise Time	t _r			13	20	
Turn-Off Delay Time	t _{d(off)}			25	40	
Fall Time	t _f			15	25	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -1.7 A, di/dt = 100 A/μs		60	90	

Notes

- a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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