BCW70LT1

General Purpose Transistors

PNP Silicon

ON Semiconductor
Formerly a Division of Motorola
http://onsemi.com

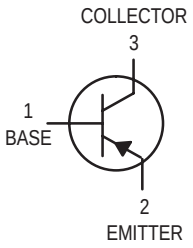
MAXIMUM RATINGS

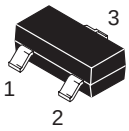
Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	–45	Vdc
Emitter–Base Voltage	V_{EBO}	–5.0	Vdc
Collector Current — Continuous	I_C	–100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board (1) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate, (2) T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	–55 to +150	°C

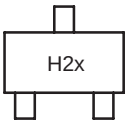
1. FR–5 = 1.0 x 0.75 x 0.062 in.
2. Alumina = 0.4 x 0.3 x 0.024 in. 99.5% alumina





SOT–23 (TO–236AB)
CASE 318
STYLE 6

DEVICE MARKING



x = Monthly Date Code

ORDERING INFORMATION

Device	Package	Shipping
BCW70LT1	SOT–23	3000 Units/Reel

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (I_C = –2.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	–45	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = –100 μAdc, V_{EB} = 0)	$V_{(BR)CES}$	–50	—	Vdc
Emitter–Base Breakdown Voltage (I_E = –10 μAdc, I_C = 0)	$V_{(BR)EBO}$	–5.0	—	Vdc
Collector Cutoff Current (V_{CB} = –20 Vdc, I_E = 0) (V_{CB} = –20 Vdc, I_E = 0, T_A = 100°C)	I_{CBO}	 — —	 –100 –10	 nAdc μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = –2.0 mAdc, V_{CE} = –5.0 Vdc)	h_{FE}	215	500	—
Collector–Emitter Saturation Voltage (I_C = –10 mAdc, I_B = –0.5 mAdc)	$V_{CE(sat)}$	—	–0.3	Vdc
Base–Emitter On Voltage (I_C = –2.0 mAdc, V_{CE} = –5.0 Vdc)	$V_{BE(on)}$	–0.6	–0.75	Vdc
SMALL–SIGNAL CHARACTERISTICS				
Output Capacitance (I_E = 0, V_{CB} = –10 Vdc, f = 1.0 MHz)	C_{obo}	—	7.0	pF
Noise Figure (I_C = –0.2 mAdc, V_{CE} = –5.0 Vdc, R_S = 2.0 kΩ, f = 1.0 kHz, BW = 200 Hz)	N_F	—	10	dB

TYPICAL NOISE CHARACTERISTICS

(V_{CE} = –5.0 Vdc, T_A = 25°C)

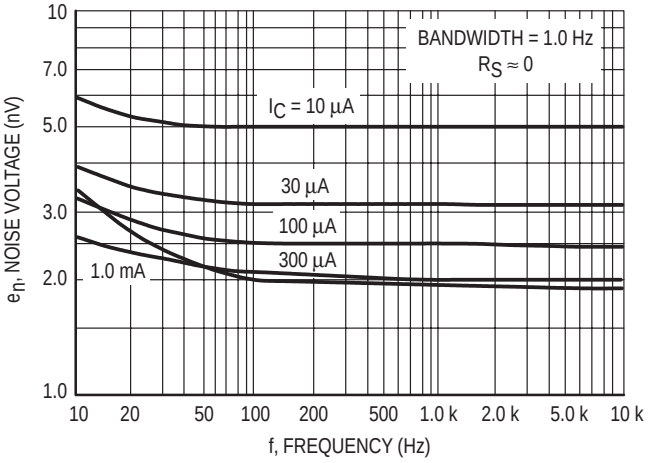


Figure 1. Noise Voltage

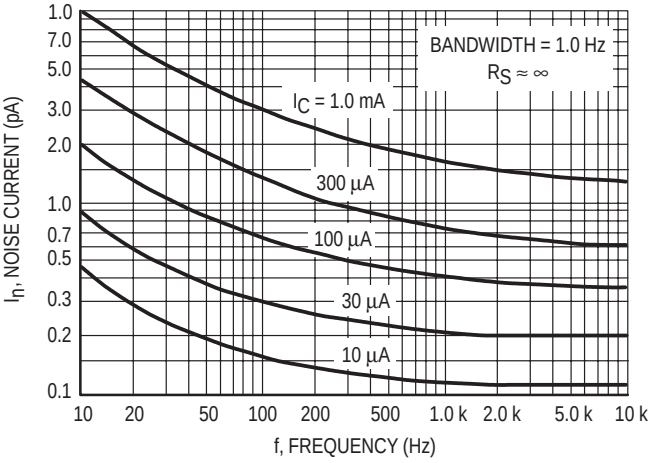


Figure 2. Noise Current

NOISE FIGURE CONTOURS

(V_{CE} = –5.0 Vdc, T_A = 25°C)

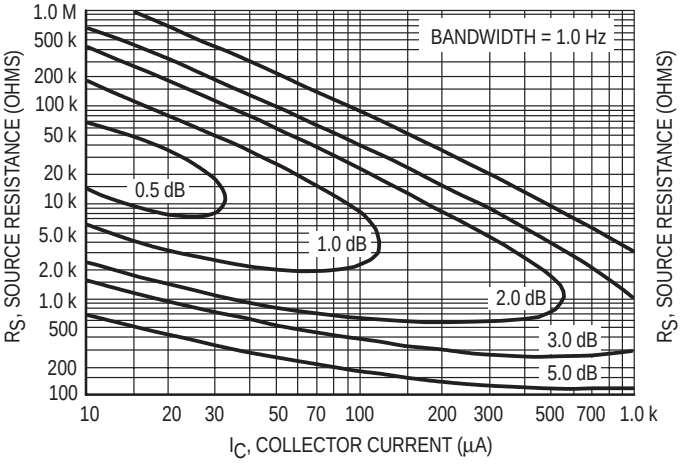


Figure 3. Narrow Band, 100 Hz

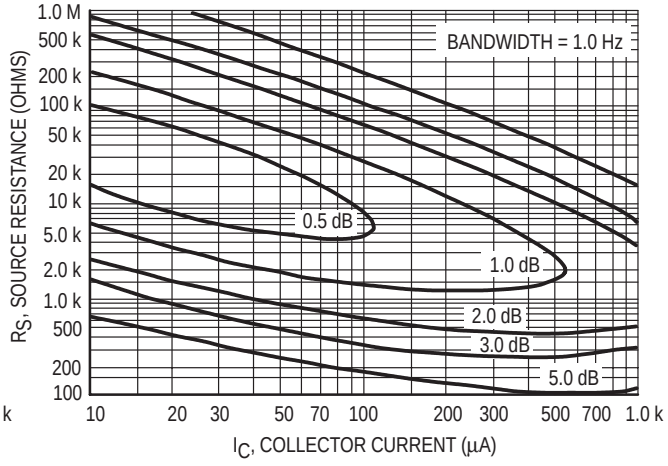


Figure 4. Narrow Band, 1.0 kHz

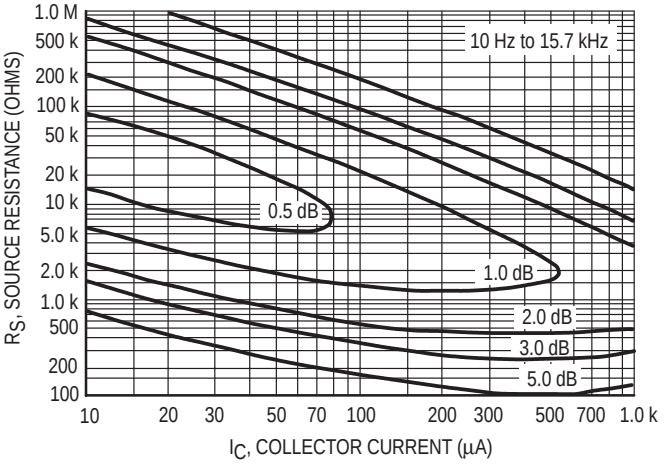


Figure 5. Wideband

Noise Figure is Defined as:

$$NF = 20 \log_{10}\left[\frac{e_n^2 + 4KTR_S + I_n{}^2R_S{}^2}{4KTR_S}\right]^{1/2}$$

e_n = Noise Voltage of the Transistor referred to the input. (Figure 3)

I_n = Noise Current of the Transistor referred to the input. (Figure 4)

K = Boltzman's Constant (1.38 x 10^{-23} j/°K)

T = Temperature of the Source Resistance (°K)

R_S = Source Resistance (Ohms)

TYPICAL STATIC CHARACTERISTICS

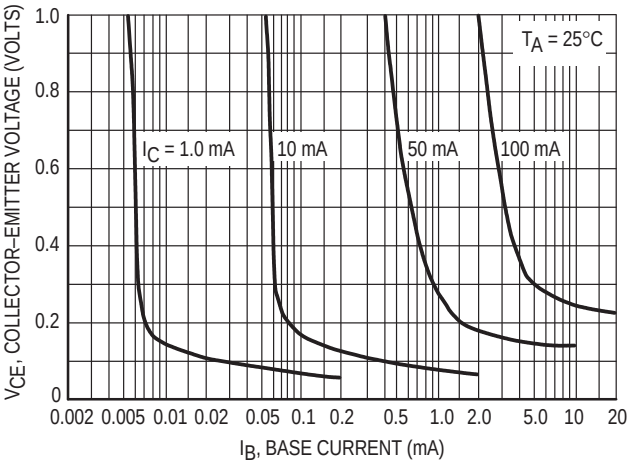


Figure 6. Collector Saturation Region

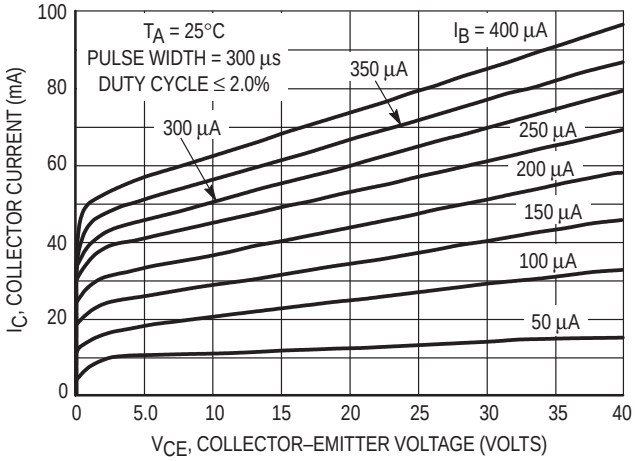


Figure 7. Collector Characteristics

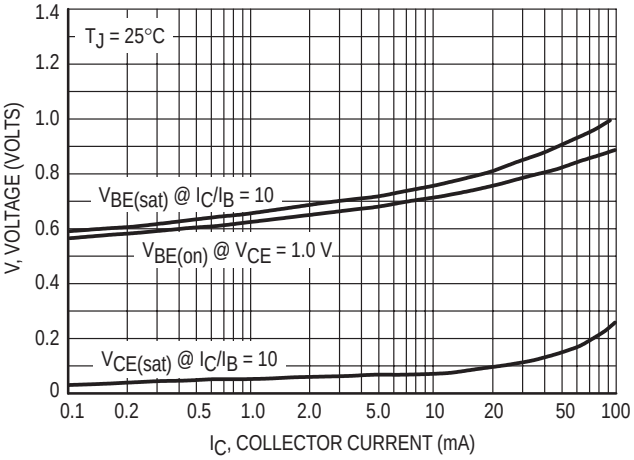


Figure 8. “On” Voltages

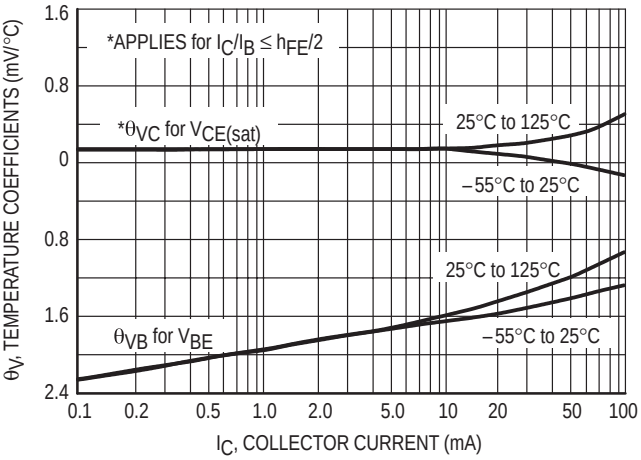


Figure 9. Temperature Coefficients

TYPICAL DYNAMIC CHARACTERISTICS

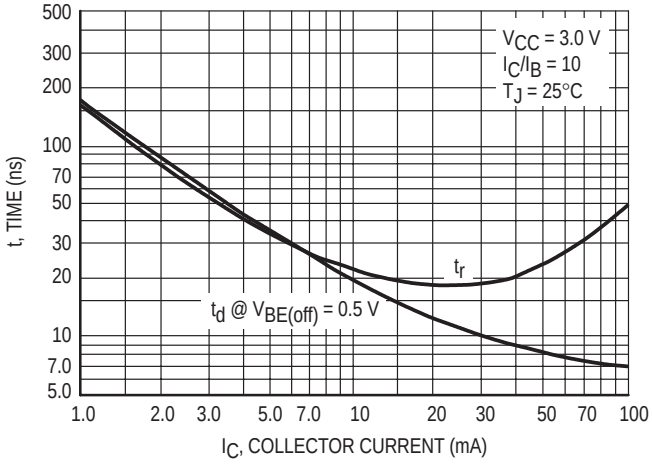


Figure 10. Turn–On Time

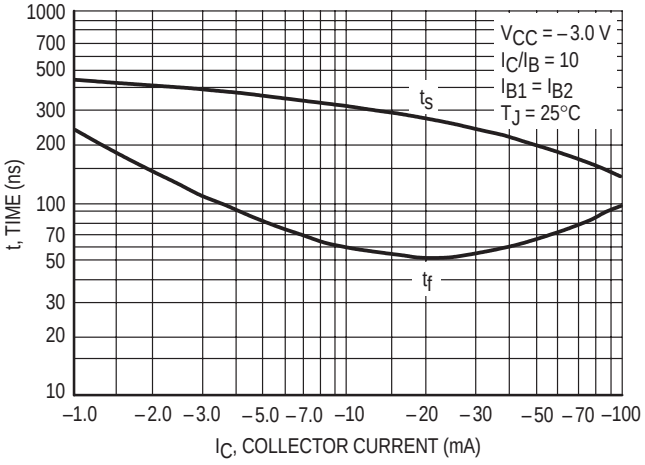


Figure 11. Turn–Off Time

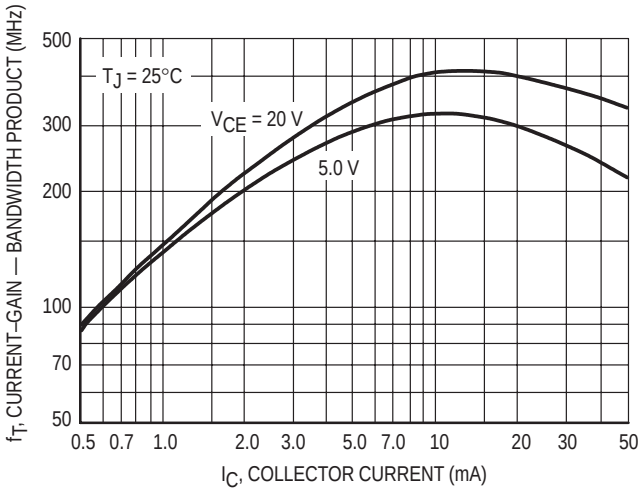


Figure 12. Current–Gain — Bandwidth Product

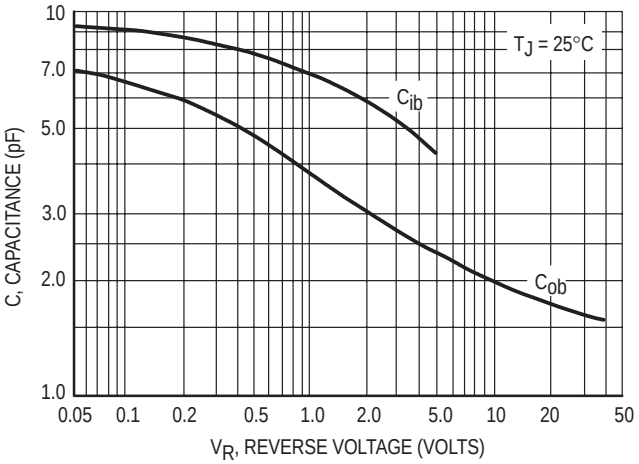


Figure 13. Capacitance

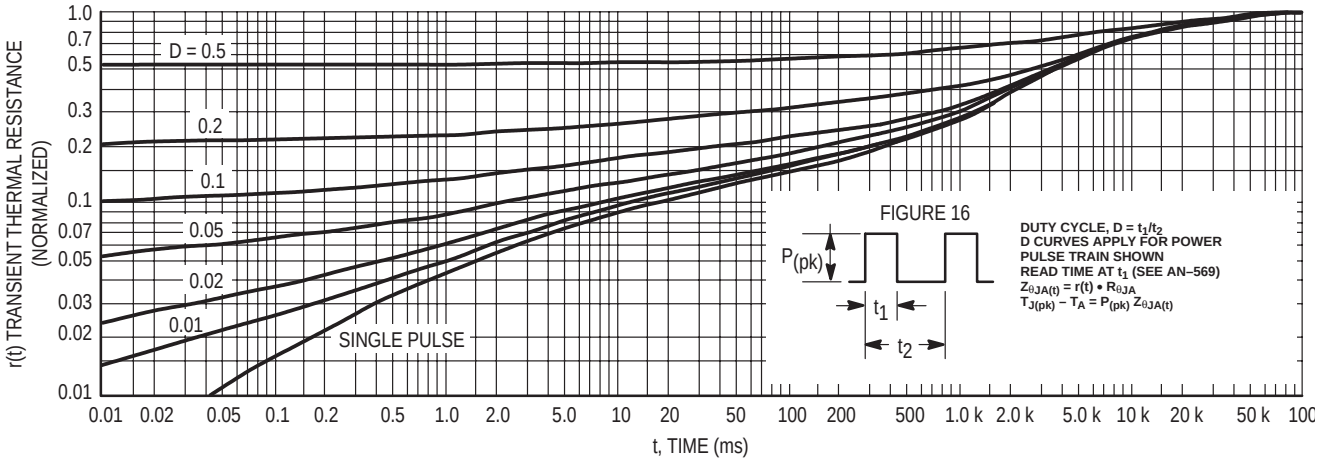


Figure 14. Thermal Response

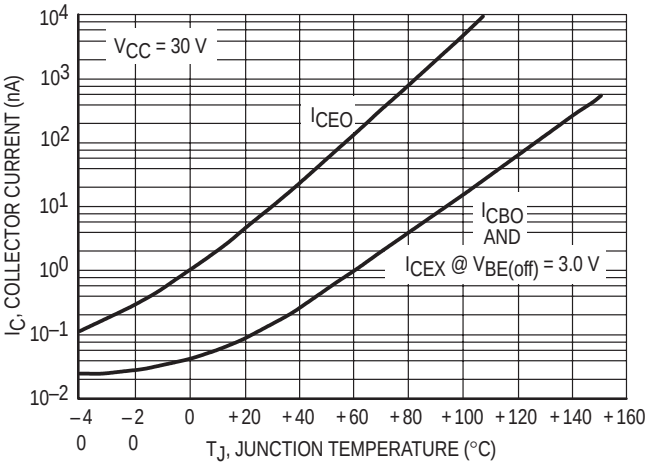


Figure 15. Typical Collector Leakage Current

DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 16. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 14 was calculated for various duty cycles.

To find $Z_{\theta JA(t)}$, multiply the value obtained from Figure 14 by the steady state value $R_{\theta JA}$.

Example:

Dissipating 2.0 watts peak under the following conditions:

t_1 = 1.0 ms, t_2 = 5.0 ms (D = 0.2)

Using Figure 14 at a pulse width of 1.0 ms and D = 0.2, the reading of r(t) is 0.22.

The peak rise in junction temperature is therefore

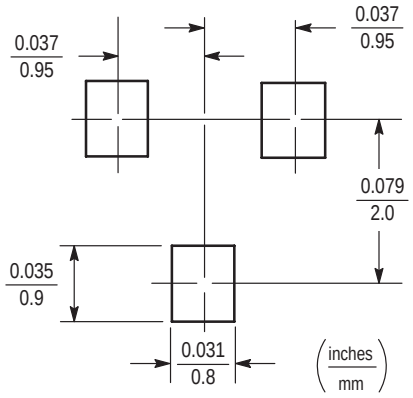
$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88°C$.

For more information, see AN–569.

INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–23

SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

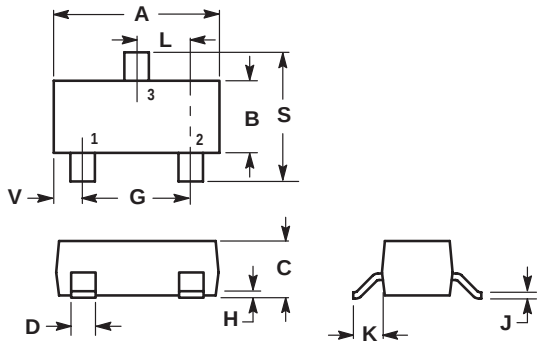
The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS

SOT–23 (TO–236AB)
CASE 318–08
ISSUE AF



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

Thermal Clad is a trademark of the Bergquist Company

PUBLICATION ORDERING INFORMATION

North America Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support
German Phone: (+1) 303–308–7140 (M–F 2:30pm to 5:00pm Munich Time)
Email: ONlit–german@hibbertco.com
French Phone: (+1) 303–308–7141 (M–F 2:30pm to 5:00pm Toulouse Time)
Email: ONlit–french@hibbertco.com
English Phone: (+1) 303–308–7142 (M–F 1:30pm to 5:00pm UK Time)
Email: ONlit@hibbertco.com

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support
Phone: 303–675–2121 (Tue–Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong 800–4422–3781
Email: ONlit–asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–8549
Phone: 81–3–5487–8345
Email: r14153@onsemi.com

Fax Response Line: 303–675–2167
800–344–3810 Toll Free USA/Canada

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local Sales Representative.