AAT4252A

SmartSwitch™

Dual Slew Rate Controlled Load Switch

General Description

The AAT4252A SmartSwitch™ is a dual P-channel MOSFET power switch designed for high-side load-switching applications. Each MOSFET has a typical $R_{DS(ON)}$ of 105mΩ, allowing increased load switch current handling capacity with a low forward voltage drop. The device is available in three different versions with flexible turn-on and turn-off characteristics–from very fast to slew-rate limited. The standard 4252A (-1) version has a slew-rate limited turn-on load switch. The AAT4252A (-2) version features a fast turn-on capabilities, typically less than 500ns turn-on and 3µs turn-off times. The AAT4252A (-3) variation offers a shutdown load discharge circuit to rapidly turn-off a load circuit when the switch is disabled. An additional feature is a slew-rate selector pin which can switch between fast and slow slew rate.

All the AAT4252A load switch versions are designed to operate from 1.5V up to 6.5V, making then ideal for both 3V and 5V systems. Input logic levels are TTL and 2.5V to 5V CMOS compatible. The quiescent supply current is a very low 500nA.

The AAT4252A is available in the Pb-free TSOPJW-12 package and is specified over the -40°C to +85°C temperature range.

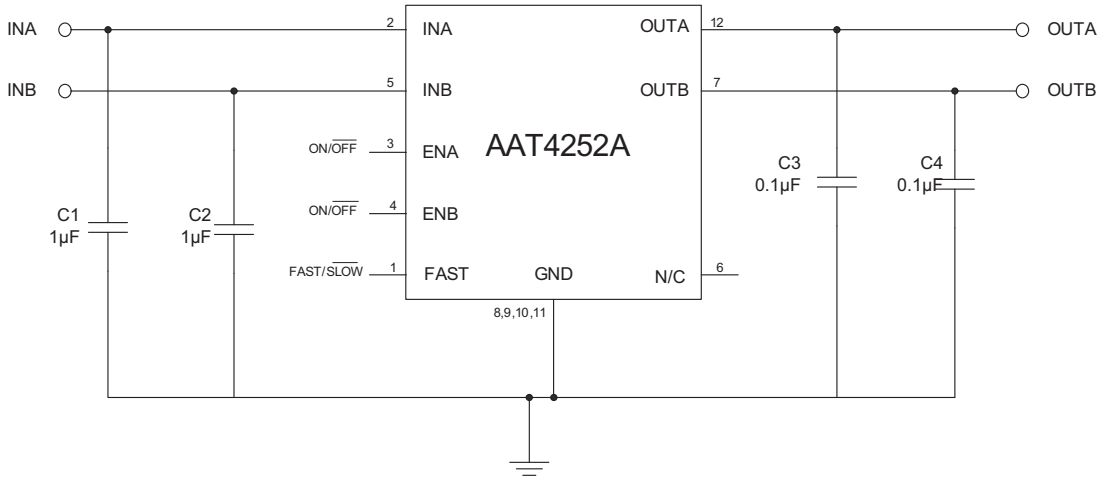
Features

- V_{IN} Range: 1.5V to 6.5V
- Low $R_{DS(ON)}$
  - 87mΩ Typical @ 5V
  - 196mΩ Typical @ 1.5V
- Slew Rate Turn-On Time Options
  - 1ms
  - 0.5µs
  - 100µs
- Fast Shutdown Load Discharge Option
- Low Quiescent Current
  - Typically 500nA
- TTL/CMOS Input Logic Level
- Temperature Range: -40°C to +85°C
- Available in TSOPJW-12 Package

Applications

- Cellular Telephones
- Digital Still Cameras
- Notebook Computers
- PDA Phones
- PDAs
- PMPs
- Smartphones

Typical Application

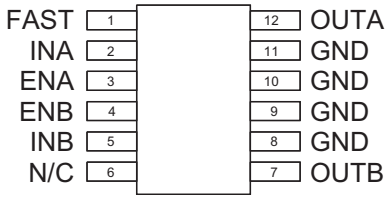


Pin Descriptions

Pin #	Symbol	Function
1	FAST	Active-high input switches between FAST (Logic H) and SLOW (Logic L) slew rate.
2	INA	This is the pin to the P-channel MOSFET source for Switch A. Bypass to ground through a 1µF capacitor. INA is independent of INB.
3	ENA	Active-High Enable Input A. A logic low turns the switch off and the device consumes less than 1µA of current. Logic high resumes normal operation.
4	ENB	Active-High Enable Input B. A logic low turns the switch off and the device consumes less than 1µA of current. Logic high resumes normal operation.
5	INB	This is the pin to the P-channel MOSFET source for Switch B. Bypass to ground through a 1µF capacitor. INB is independent of INA.
6	N/C	Not connected.
7	OUTB	This is the pin to the P-channel MOSFET drain connection. Bypass to ground through a 0.1µF capacitor.
8, 9, 10, 11	GND	Ground connection.
12	OUTA	This is the pin to the P-channel MOSFET drain connection. Bypass to ground through a 0.1µF capacitor.

Pin Configuration

TSOPJW-12
(Top View)



Selector Guide

Part Number	Slew Rate (Typ)		Active Pull-Down	Enable
	FAST (H)	SLOW (L)		
AAT4252A-1[1]	1ms		NO	Active High
AAT4252A-2[1]	0.5µs		NO	Active High
AAT4252A-3	100µs	1ms	YES	Active High

Absolute Maximum Ratings[2]

Symbol	Description		Value	Units
V_{IN}	IN to GND		-0.3 to 7	V
V_{EN}, FAST	EN, FAST to GND		-0.3 to 7	V
V_{OUT}	OUT to GND		-0.3 to V_{IN} + 0.3	V
I_{MAX}	Maximum Continuous Switch Current		1.8	A
I_{DM}	Maximum Pulsed Current	IN ≥ 2.5V	5.5	A
		IN ≤ 2.5V	2.0	
T_J	Operating Junction Temperature Range		-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads)		300	°C
V_{ESD}	ESD Rating[3] - HBM		4000	V

Thermal Characteristics[4]

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance	160	°C/W
P_D	Maximum Power Dissipation	625	mW

1. Contact Sales for product availability
2. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
3. Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
4. Mounted on an AAT4252A demo board in still 25°C air.

Electrical Characteristics[1]

V_{IN} = 5V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = 25°C per channel.

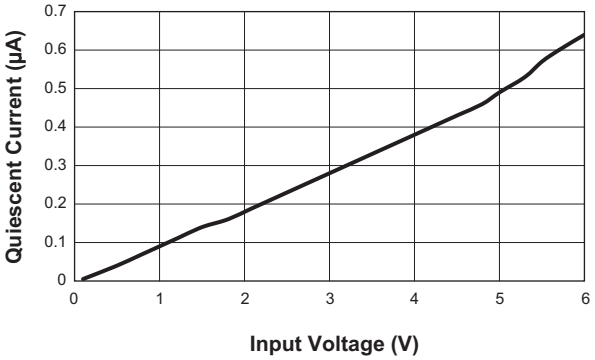
Symbol	Description	Conditions	Min	Typ	Max	Units
AAT4252A All Versions						
V_{IN}	Operation Voltage		1.5		6.5	V
I_Q	Quiescent Current	ON/OFF = ACTIVE, FAST = V_{IN}, I_{OUT} = 0			1.0	µA
$I_{Q(OFF)}$	Off Supply Current	ON/OFF = Inactive, OUT = Open			1.0	µA
$I_{SD(OFF)}$	Off Switch Current[2]	ON/OFF = GND, V_{OUT} = 0			1.0	µA
$R_{DS(ON)}$	On-Resistance	V_{IN} = 5V		87	155	mΩ
		V_{IN} = 4.2V		92		
		V_{IN} = 3.0V		103		
		V_{IN} = 1.8V		145		
		V_{IN} = 1.5V		196		
TCR_{RDS}	On Resistance Temperature Coefficient			2800		ppm/°C
V_{IL}	ON/OFF Input Logic Low Voltage	V_{IN} = 1.5V to 5.5V			0.4	V
V_{IH}	ON/OFF Input Logic High Voltage	V_{IN} = 1.5V to 5.5V	1.4			V
I_{SINK}	ON/OFF Input Leakage	$V_{ON/OFF}$ = 5.5V			1.0	µA
AAT4252A-1[2]						
$T_{D(ON)}$	Output Turn-On Delay Time	V_{IN} = 5V, R_{LOAD} =10Ω, T_A = 25°C		10	40	µs
T_{ON}	Turn-On Rise Time	V_{IN} = 5V, R_{LOAD} =10Ω, T_A = 25°C		600	1500	µs
$T_{D(OFF)}$	Output Turn-OFF Delay Time	V_{IN} = 5V, R_{LOAD} =10Ω, T_A = 25°C		2.0	10	µs
AAT4252A-2[2]						
$T_{D(ON)}$	Output Turn-On Delay Time	V_{IN} = 5V, R_{LOAD} =10Ω, T_A = 25°C		0.5	2	µs
T_{ON}	Turn-On Rise Time	V_{IN} = 5V, R_{LOAD} =10Ω, T_A = 25°C		0.5	1.0	µs
$T_{D(OFF)}$	Output Turn-OFF Delay Time	V_{IN} = 5V, R_{LOAD} =10Ω, T_A = 25°C		4.0	10	µs
AAT4252A-3						
$T_{D(ON)}$	Output Turn-On Delay Time	V_{IN} = 5V, R_{LOAD} =10Ω, T_A = 25°C		10	40	µs
T_{ON}	Turn-On Rise Time	V_{IN} = 5V, R_{LOAD} =10Ω, FAST = 5V, T_A = 25°C		65	150	µs
T_{ON}	Turn-On Rise Time	V_{IN} = 5V, R_{LOAD} =10Ω, FAST = 0V, T_A = 25°C		600	1500	µs
$T_{D(OFF)}$	Output Turn-OFF Delay Time	V_{IN} = 5V, R_{LOAD} =10Ω, T_A = 25°C		2.0	10	µs
R_{PD}	Output Pull-Down Resistance During OFF	ON/OFF = Inactive, T_A = 25°C		10	50	Ω

1. The AAT4252A is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.
2. Contact Sales for product availability.

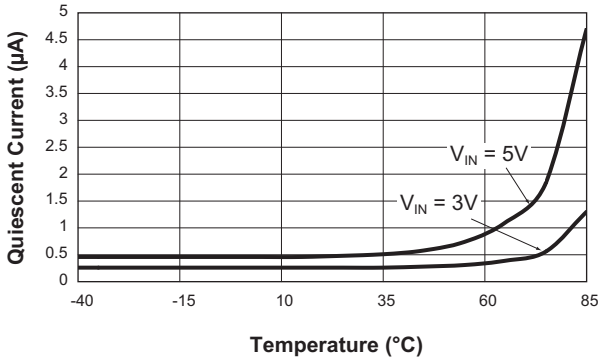
Typical Characteristics

V_{IN} = 5V, T_A = 25°C unless otherwise noted.

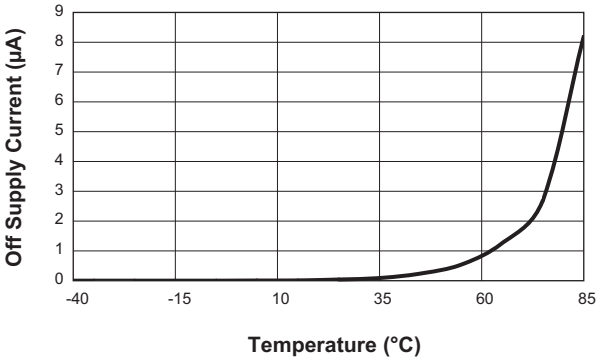
Quiescent Current vs. Input Voltage
(No Load; Single Switch)



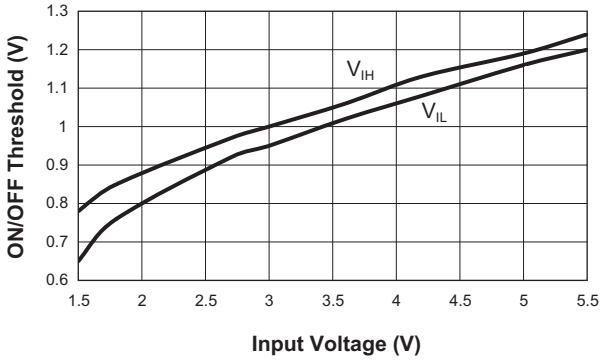
Quiescent Current vs. Temperature
(No Load; Single Switch)



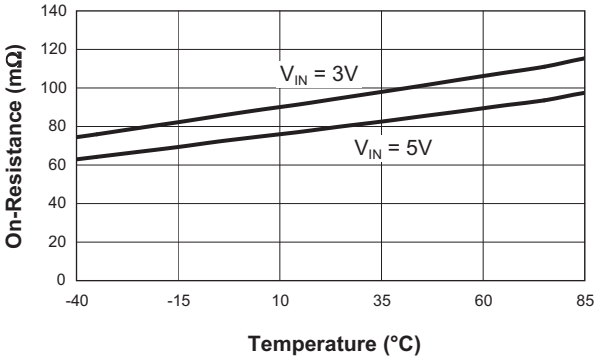
Off Supply Current vs. Temperature
(No Load; EN = GND; V_{IN} = 5V)



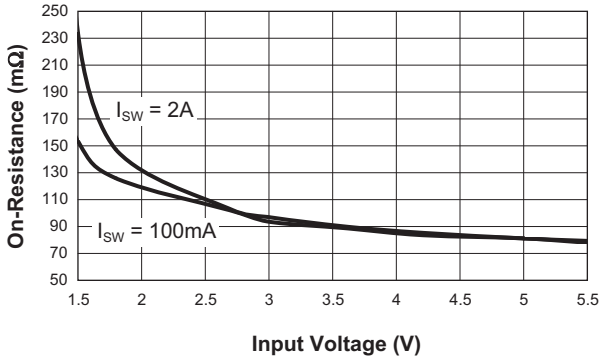
Typical ON/OFF Threshold vs. Input Voltage



On-Resistance vs. Temperature



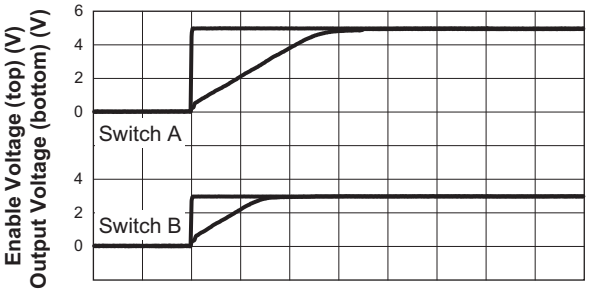
On-Resistance vs. Input Voltage



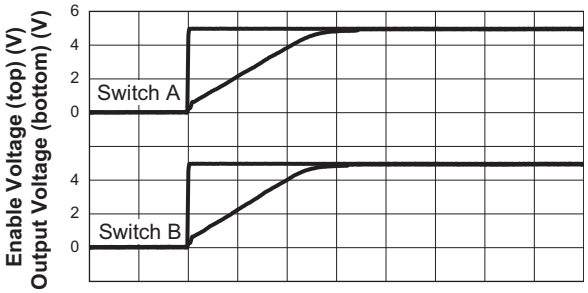
Typical Characteristics

V_{IN} = 5V, T_A = 25°C unless otherwise noted.

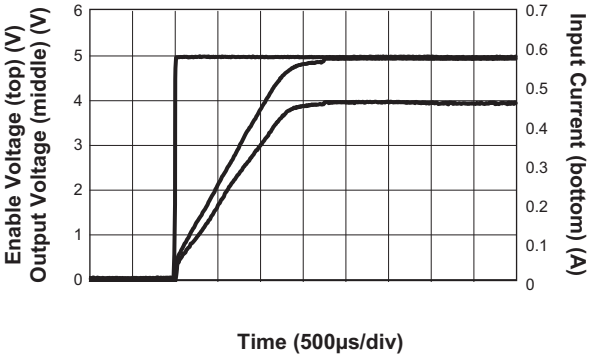
Output Turn-On
(V_{INA}/V_{ENA} = 5V; V_{INB}/V_{ENB} = 3V; R_{LA} = 10Ω; R_{LB} = 20Ω)



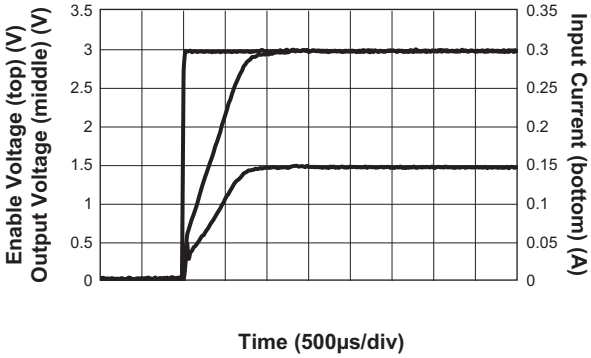
Output Turn-On
($V_{INA}/V_{INB}/V_{EN}$ = 5V; R_L = 10Ω)



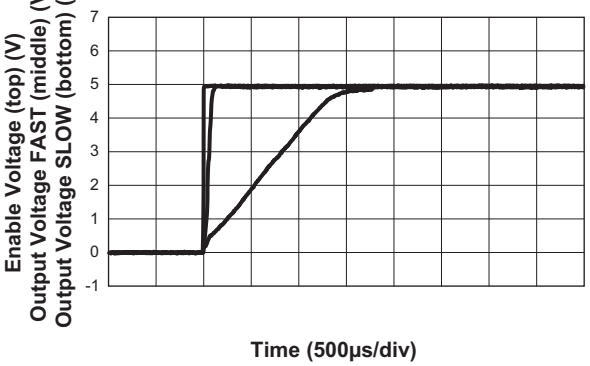
Output Turn-On
(V_{IN} = 5V; R_L = 10Ω)



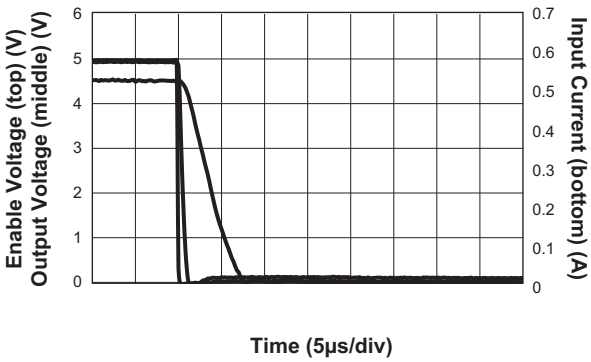
Output Turn-On
(V_{IN} = 3V; R_L = 20Ω)



Output Turn-On
(R_L = 10Ω)



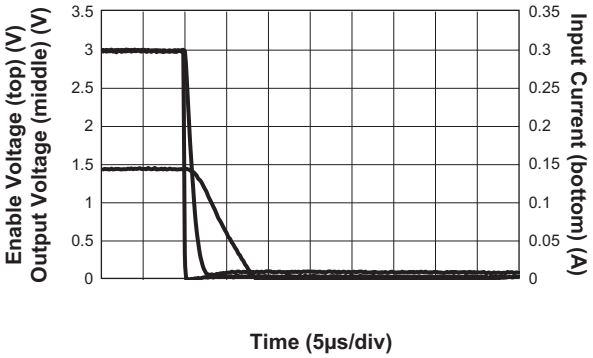
Output Turn-Off
(V_{IN} = 5V; R_L = 10Ω)



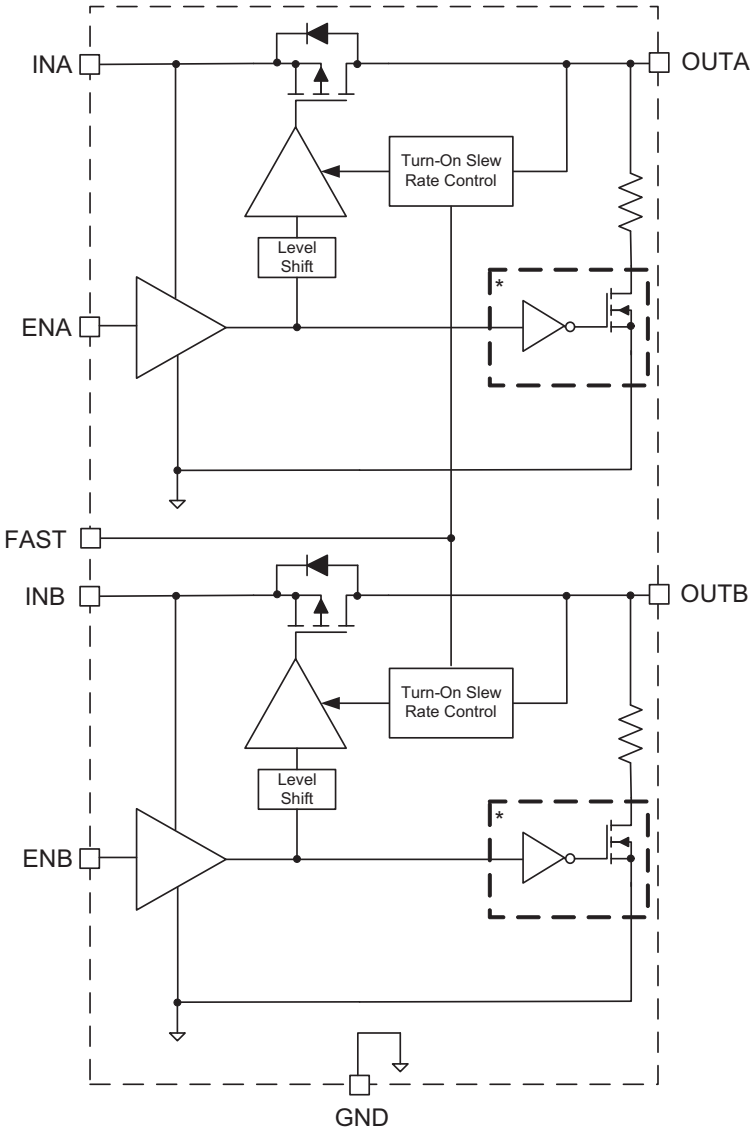
Typical Characteristics

V_{IN} = 5V, T_A = 25°C unless otherwise noted.

Output Turn-Off
(V_{IN} = 3V; R_L = 20Ω)



Functional Block Diagram



*AAT4252A-3 version only

Functional Description

The AAT4252A is a family of flexible dual P-channel MOSFET power switches designed for high-side load switching applications. There are three versions of the AAT4252A with different turn-on and turn-off characteristics to choose from, depending upon the specific requirements of an application.

The first version, the AAT4252A-1, has a moderate turn-on slew rate feature, which reduces in-rush current when the MOSFET is turned on. This function allows the load switch to be implemented with either a small input capacitor or no input capacitor at all. During turn-on slewing, the current ramps linearly until it reaches the level required for the output load condition. The proprietary turn-on current control method works by careful control and monitoring of the MOSFET gate voltage. When the device is switched ON, the gate voltage is quickly increased to the threshold level of the MOSFET. Once at this level, the current begins to slew as the gate voltage is slowly increased until the MOSFET becomes fully enhanced. Once it has reached this point the gate is quickly increased to the full input voltage and the $R_{DS(ON)}$ is minimized.

The second version, the AAT4252A-2, is a very fast switch intended for high-speed switching applications. This version has no turn-on slew rate control and no special output discharge features.

The final switch version, the AAT4252A-3, has the addition of a minimized slew rate limited turn-on function and a shutdown output discharge circuit to rapidly turn off a load when the load switch is disabled through the ON/OFF pin. Using the FAST input pin on the AAT4252A-3, the device can be manually switched to a slower slew rate.

All versions of the AAT4252A operate with input voltages ranging from 1.5V to 6.5V. All versions of this device have extremely low operating current, making them ideal for battery-powered applications.

The ON/OFF control pin is TTL compatible and will also function with 2.5V to 5V logic systems, making the AAT4252A an ideal level-shifting load switch.

Applications Information

Input Capacitor

A 1µF or larger capacitor is typically recommended for C_{IN} in most applications. A C_{IN} capacitor is not required for basic operation; however, it is useful in preventing load transients from affecting upstream circuits. C_{IN} should be located as close to the device VIN pin as practically possible. Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN}. There is no specific capacitor equivalent series resistance (ESR) requirement for C_{IN}. However, for higher current C_{IN}, ceramic capacitors are recommended for CIN due to their inherent capability over tantalum capacitors to withstand input current surges from low-impedance sources, such as batteries in portable devices.

Output Capacitor

For proper slew operation, a 0.1µF capacitor or greater is required between V_{OUT} and GND. Likewise, with the output capacitor, there is no specific capacitor ESR requirement. If desired, C_{OUT} may be increased without limit to accommodate any load transient condition without adversely affecting the slew rate.

Enable Function

The AAT4252A features an enable / disable function. This pin (ON) is active high and is compatible with TTL or CMOS logic. To assure the load switch will turn on, the ON control level must be greater than 2.0V. The load switch will go into shutdown mode when the voltage on the ON pin falls below 0.8V. When the load switch is in shutdown mode, the OUT pin is tri-stated, and quiescent current drops to leakage levels below 1µA.

Reverse Output-to-Input Voltage Conditions and Protection

Under normal operating conditions, a parasitic diode exists between the output and input of the load switch. The input voltage should always remain greater than the output load voltage, maintaining a reverse bias on the internal parasitic diode. Conditions where V_{OUT} might exceed V_{IN} should be avoided since this would forward bias the internal parasitic diode and allow excessive current flow into the V_{OUT} pin, possibly damaging the load switch. In applications where there is a possibility of V_{OUT} exceeding V_{IN} for brief periods of time during normal operation, the use of a larger value C_{IN} capacitor is

highly recommended. A larger value of C_{IN} with respect to C_{OUT} will effect a slower C_{IN} decay rate during shutdown, thus preventing V_{OUT} from exceeding V_{IN}. In applications where there is a greater danger of V_{OUT} exceeding V_{IN} for extended periods of time, it is recommended to place a Schottky diode from V_{IN} to V_{OUT} (connecting the cathode to V_{IN} and anode to V_{OUT}). The Schottky diode forward voltage should be less than 0.45V.

Thermal Considerations and High Output Current Applications

The AAT4252A is designed to deliver a continuous output load current. The limiting characteristic for maximum safe operating output load current is package power dissipation. In order to obtain high operating currents, careful device layout and circuit operating conditions must be taken into account.

The following discussions will assume the load switch is mounted on a printed circuit board utilizing the minimum recommended footprint as stated in the Printed Circuit Board Layout Recommendations section of this datasheet.

At any given ambient temperature (T_A), the maximum package power dissipation can be determined by the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Constants for the AAT4252A are maximum junction temperature ($T_{J(MAX)}$ = 125°C[1]) and package thermal resistance (θ_{JA} = 160°C/W). Worst case conditions are calculated at the maximum operating temperature, T_A = 85°C. Typical conditions are calculated under normal ambient conditions where T_A = 25°C. At T_A = 85°C, $P_{D(MAX)}$ = 250mW. At T_A = 25°C, $P_{D(MAX)}$ = 625mW.

The maximum continuous output current for the AAT4252A is a function of the package power dissipation and the R_{DS} of the MOSFET at $T_{J(MAX)}$. The maximum R_{DS} of the MOSFET at $T_{J(MAX)}$ is calculated by increasing the maximum room temperature R_{DS} by the R_{DS} temperature coefficient. The temperature coefficient (T_C) is 2800ppm/°C. Therefore, at 125°C:

$R_{DS(MAX)} = R_{DS(25°C)} \cdot (1 + T_C \cdot \Delta T)$
$R_{DS(MAX)} = 155m\Omega \cdot (1 + 0.002800 \cdot (125°C - 25°C))$
$R_{DS(MAX)} = 198m\Omega$

For maximum current, refer to the following equation:

$$I_{OUT(MAX)} < \sqrt{\frac{P_{D(MAX)}}{R_{DS}}}$$

For example, if V_{IN} = 5V, $R_{DS(MAX)}$ = 198mΩ, and T_A = 25°C, $I_{OUT(MAX)}$ = 1.8A. If the output load current were to exceed 1.8A or if the ambient temperature were to increase, the internal die temperature would increase and the device would be damaged. Higher peak currents can be obtained with the AAT4252A. To accomplish this, the device thermal resistance must be reduced by increasing the heat sink area or by operating the load switch in a duty cycle manner. Duty cycles with peaks less than 2ms in duration can be considered using the method below.

High Peak Output Current Applications

Some applications require the load switch to operate at a continuous nominal current level with short duration, high-current peaks. Refer to the I_{DM} specification in the Absolute Maximum Ratings table to ensure the AAT4252A's maximum pulsed current rating is not exceeded. The duty cycle for both output current levels must be taken into account. To do so, first calculate the power dissipation at the nominal continuous current level, and then add the additional power dissipation due to the short duration, high-current peak scaled by the duty factor. For example, a 4V system using an AAT4252A operates at a continuous 100mA load current level and has short 2A current peaks, as in a GSM application. The current peak occurs for 576µs out of a 4.61ms period.

First, the current duty cycle is calculated:

$$\%\ \text{Peak Duty Cycle} = \left(\frac{x}{100}\right) = \left(\frac{576\mu s}{4.61ms}\right)$$

$$\%\ \text{Peak Duty Cycle} = 12.5\%$$

1. The actual maximum junction temperature of AAT4252A is 150°C. However, good design practice is to derate the maximum die temperature down to 125°C to prevent the possibility of over temperature damage.

The load current is 100mA for 87.5% of the 4.61ms period and 2A for 12.5% of the period. Since the Electrical Characteristics do not report $R_{DS(MAX)}$ for 4V operation, it must be approximated by consulting the chart of $R_{DS(ON)}$ vs. V_{IN}. The R_{DS} reported for 5V at 100mA and 2A can be scaled by the ratio seen in the chart to derive the R_{DS} for 4V V_{IN} at 25°C : 155mΩ · 90mΩ/87mΩ = 160.3mΩ. De-rated for temperature: 160.3mΩ · (1 + 0.002800 · (125°C -25°C)) = 205mΩ. The power dissipation for a 100mA load is calculated as follows:

$P_{D(MAX)} = I_{OUT}^2 \cdot R_{DS}$
$P_{D(100mA)} = (100mA)^2 \cdot 205m\Omega$
$P_{D(100mA)} = 2.05mW$
$P_{D(87.5\%D/C)} = \%DC \cdot P_{D(100mA)}$
$P_{D(87.5\%D/C)} = 0.875 \cdot 2.05mW$
$P_{D(87.5\%D/C)} = 1.8mW$

The power dissipation for 100mA load at 87.5% duty cycle is 1.97mW. Now the power dissipation for the remaining 12.5% of the duty cycle at 2A is calculated:

$P_{D(MAX)} = I_{OUT}^2 \cdot R_{DS}$
$P_{D(2A)} = (2A)^2 \cdot 205m\Omega$
$P_{D(2A)} = 820.97mW$
$P_{D(12.5\%D/C)} = \%DC \cdot P_{D(2A)}$
$P_{D(12.5\%D/C)} = 0.125 \cdot 820.97mW$
$P_{D(12.5\%D/C)} = 102.6mW$

The power dissipation for 2A load at 12.5% duty cycle is 102.6mW. Finally, the two power figures are summed to determine the total true power dissipation under the varied load.

$P_{D(total)} = P_{D(100mA)} + P_{D(2A)}$
$P_{D(total)} = 1.8mW + 102.6mW$
$P_{D(total)} = 104.4mW$

The maximum power dissipation for the AAT4252A operating at an ambient temperature of 85°C is 250mW. The device in this example will have a total power dissipation of 104.4mW. This is well within the thermal limits for safe operation of the device; in fact, at 85°C, the AAT4252A will handle a 2A pulse for up to 30% duty cycle. At lower ambient temperatures, the duty cycle can be further increased.

Printed Circuit Board Layout Recommendations

For proper thermal management, and to take advantage of the low $R_{DS(ON)}$ of the AAT4252A, a few circuit board layout rules should be followed: V_{IN} and V_{OUT} should be routed using wider than normal traces, and GND should be connected to a ground plane. For best performance, C_{IN} and C_{OUT} should be placed close to the package pins.

Evaluation Board Layout

The AAT4252A evaluation layout follows the printed circuit board layout recommendations and can be used for good applications layout. Refer to Figures 1 and 2.

Note: Board layout shown is not to scale.

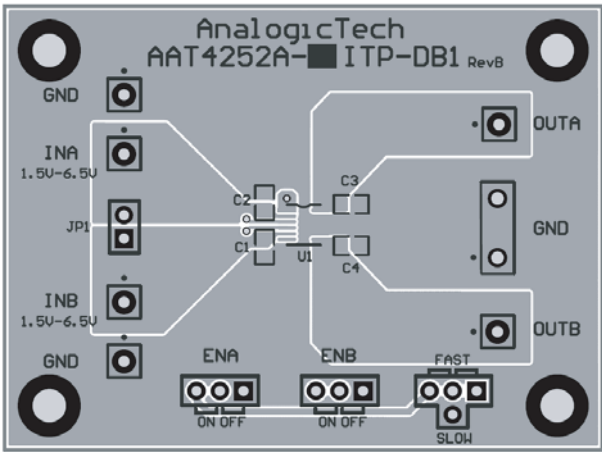


Figure 1: AAT4252A Evaluation Board Top Side Layout.

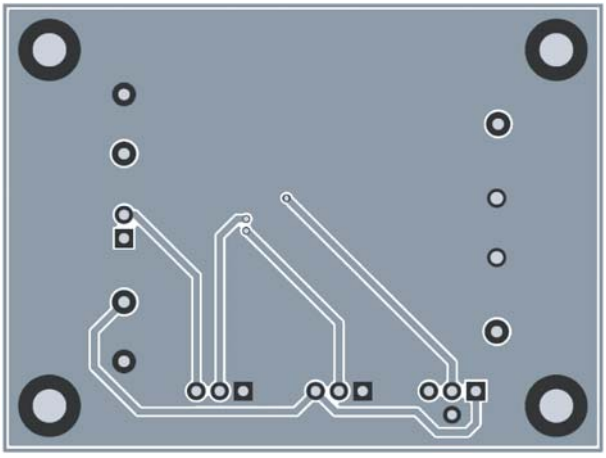


Figure 2: AAT4252A Evaluation Board Bottom Side Layout.

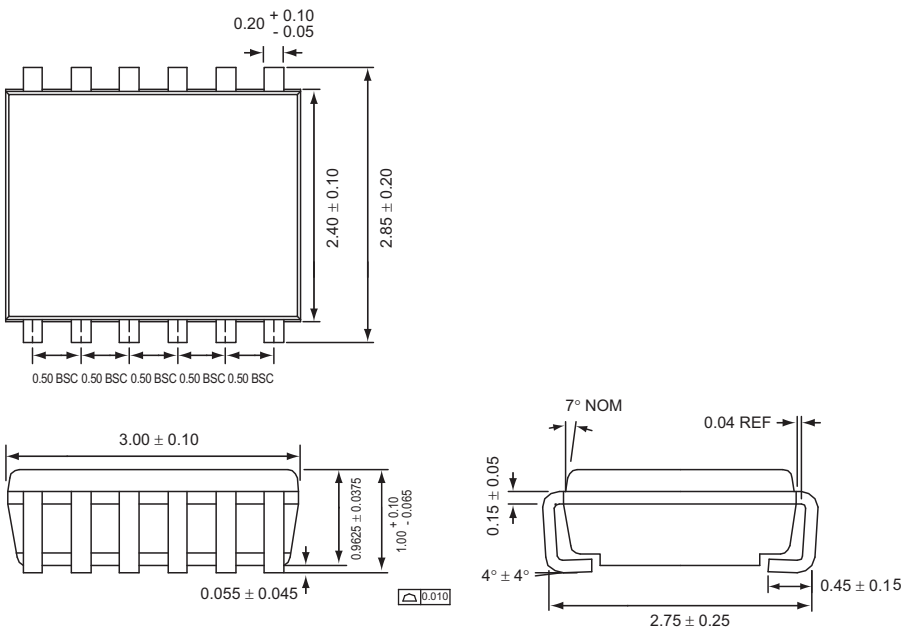
Ordering Information

Device Option	Package	Marking[1]	Part Number (Tape and Reel)[2]
AAT4252A-3	TSOPJW-12	WSXYY	**AAT4252AITP-3-T1**

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/about/quality.aspx.

Package Information

TSOPJW-12



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

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