M62376GP

8-bit 12ch D/A Converter IC Built-in 12-bit I/O Expander

REJ03D0881-0300
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Description

The M62376GP is a semiconductor IC that adopts a CMOS structure having 12 channels of 8-bit D/A converter and 12-bit I/O expander. The IC has achieved a wide operation range of 2.7 to 5.5 V in power voltage.

Data is easily available via 3-wire combination system serial input of SI, CLK and $\overline{EN}$. The IC also provides an SO pin enabling cascade connection. It provides 8 pins that share D/A converter and I/O ports that can be arbitrarily switched with serial input data.

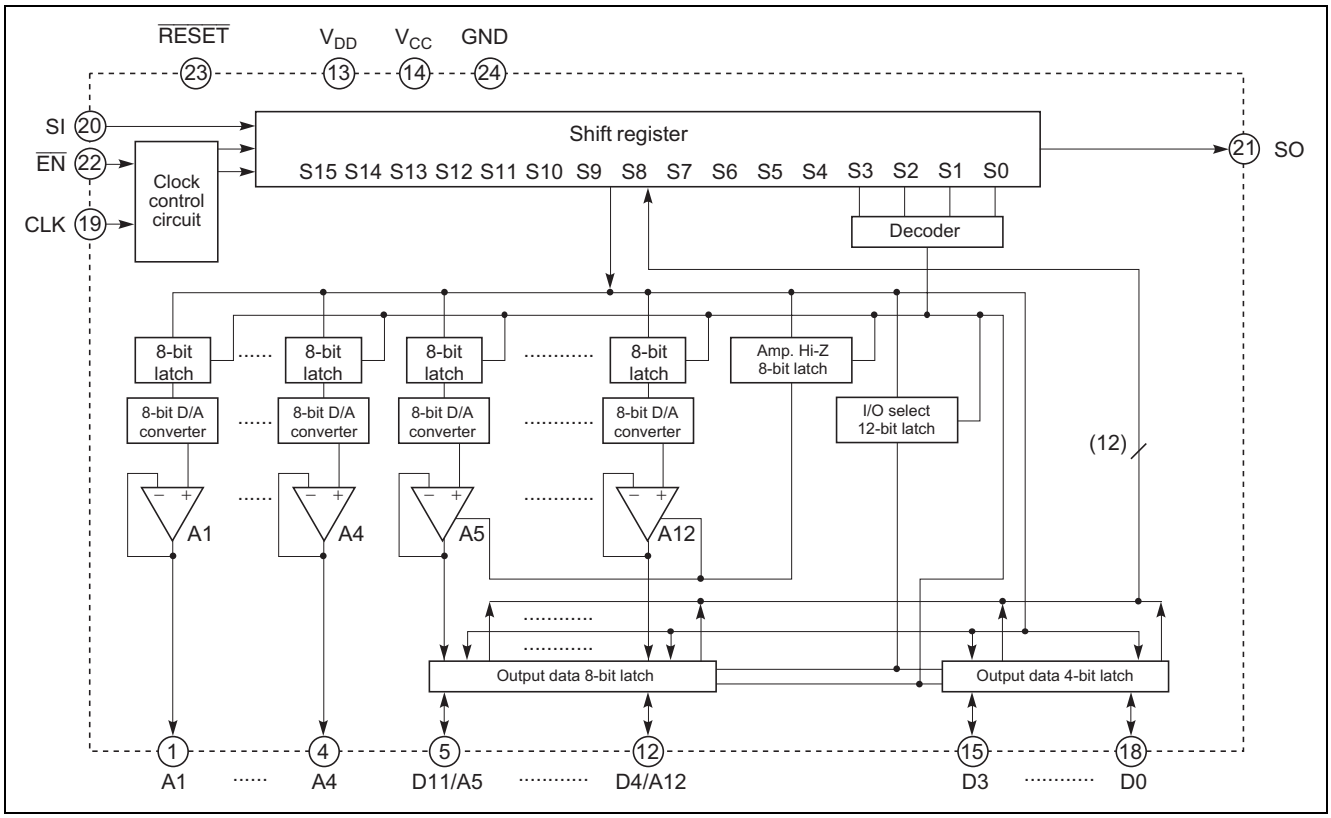
Features

- Supply voltage: 2.7 to 5.5 V
- Adopts 4 special ports for each of DAC and I/O and 8 ports that share DAC output and I/O
- Each port can be set by serial data for input/output status
- Built-in power-on reset where D/A output is set to "L" in the initial status and I/O goes to high-impedance when power is turned on
- Small package of 0.65 mm pitch and 24 pin

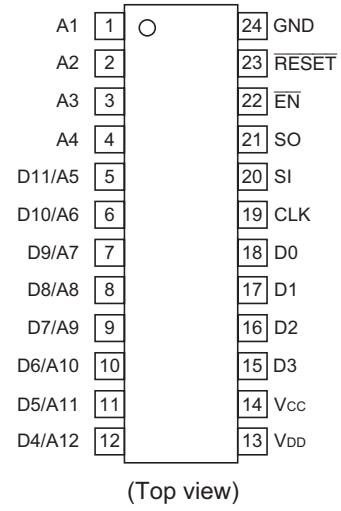
Application

Adjustment/control of industrial or home-use electronic equipment, such as VCR camera, VCR set, TV, and CRT display.

Block Diagram



Pin Arrangement



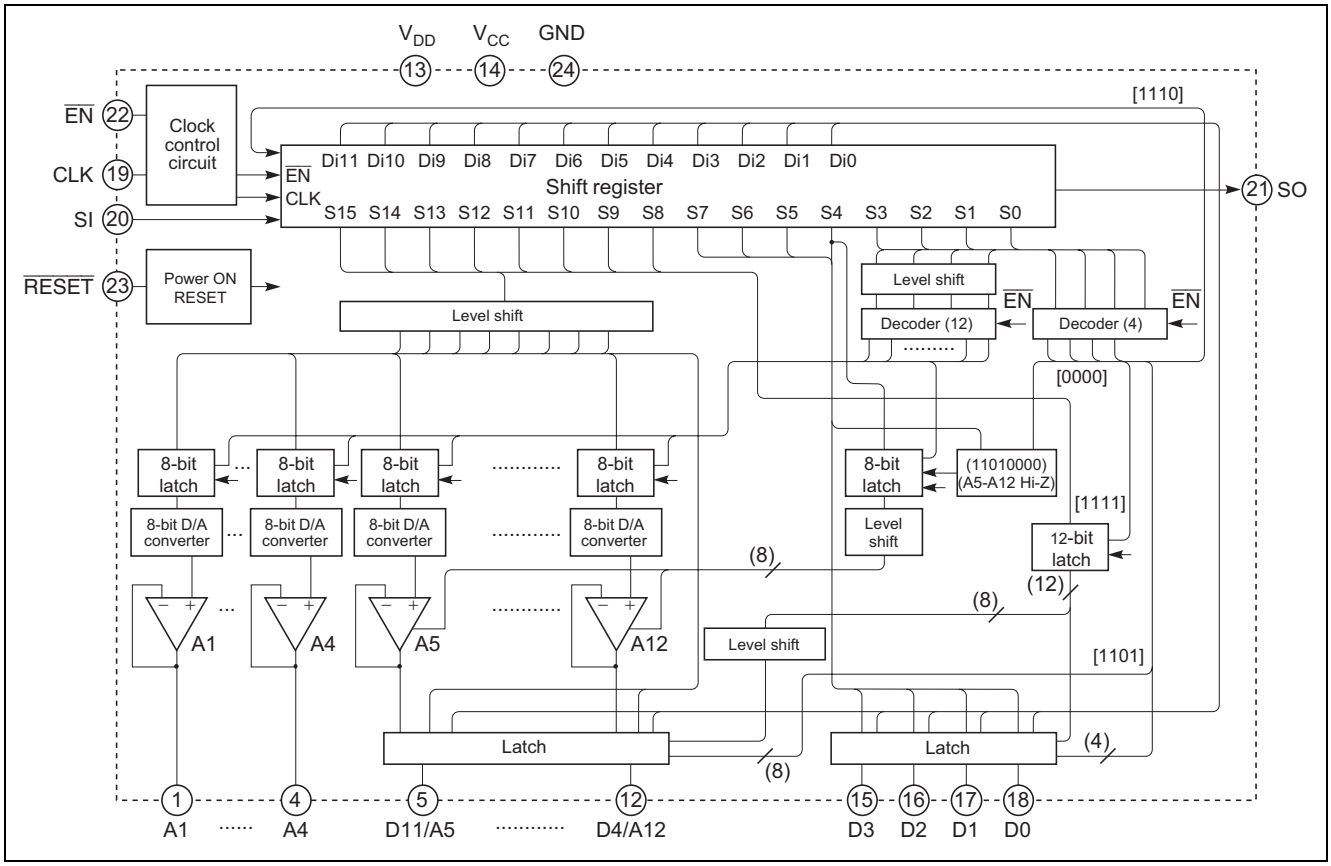
(Top view)

Outline: PLSP0024JA-A (24P2E-A)

Pin Description

Pin No.	Pin Name	Function
20	SI	Serial data input pin. Enters serial data of 16-bit in length.
21	SO	Outputs data from 16-bit shift register that reads serial data or parallel data.
19	CLK	Shift clock input pin. At the rise of shift clock, input signal from the SI pin is entered into the 16-bit shift register.
22	$\overline{EN}$	Entry of low level into the $\overline{EN}$ pin starts to read data. Putting 16-bit data at high level after input loads the input data to a specified register.
1	A1	Special output pin for 8-bit D/A converter (DAC)
2	A2	
3	A3	
4	A4	
5	D11/A5	Pin that shares I/O and DAC output. Settings can be selected with serial data. D4 to D11 are connected to the V_{DD} power supply.
6	D10/A6	
7	D9/A7	
8	D8/A8	
9	D7/A9	
10	D6/A10	
11	D5/A11	
12	D4/A12	
18	D0	Digital input output pin.
17	D1	
16	D2	
15	D3	
14	V_{CC}	Digital block power supply pin.
24	GND	GND pin
13	V_{DD}	Power supply pin in analog block and reference voltage input pin on the upper side of D/A converter
23	$\overline{RESET}$	$\overline{RESET}$ pin

Block Diagram for Explanation of Terminals



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Digital supply voltage	V_{CC}	–0.3 to +7.0	V	
Analog supply (D/A converter upper reference voltage)	V_{DD}	–0.3 to +7.0	V	
Input voltage	V_{IN}	–0.3 to V_{CC} + 0.3	V	V_{CC} supply side pin
Output voltage	Vout	–0.3 to V_{CC} + 0.3	V	V_{CC} supply side pin
Input voltage	V_{IN}	–0.3 to V_{DD} + 0.3	V	V_{DD} supply side pin
Output voltage	Vout	–0.3 to V_{DD} + 0.3	V	V_{DD} supply side pin
Power dissipation	Pd	200	mW	
Operating temperature	Topr	–20 to +85	°C	
Storage temperature	Tstg	–40 to +125	°C	

Electrical Characteristics

<Recommended Operating Condition>

Item	Symbol	Ratings	Unit	Conditions
Digital supply voltage	V_{CC}	2.7 to 5.5	V	
Analog supply (D/A converter upper reference voltage)	V_{DD}	2.7 to 5.5	V	$V_{DD} \geq V_{CC}$
Input pin voltage (V_{CC} part)	V_{IN}	0 to V_{CC}	V	$\overline{EN}$, SI, D0 to D3
Output pin voltage (V_{CC} part)	V_{OUT}	0 to V_{CC}	V	SO, D0 to D3
Input pin voltage (V_{DD} part)	V_{IN}	0 to V_{DD}	V	$\overline{RESET}$, D4/A12 to D11/A5
Output pin voltage (V_{DD} part)	V_{OUT}	0 to V_{DD}	V	A1 to A4, D4/A12 to D11/A5

<Digital Part (V_{CC}) >

(V_{CC} = 2.7 to 5.5 V, Ta = –20 to +85°C, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	V_{CC}	2.7	3.0	5.5	V	
Supply current	I_{CC}	—	0.2	2.5	mA	CLK = 1 MHz operation, V_{CC} = 3 V, I_{AO} = 0 µA
Input leak current	I_{ILK}	–10	—	10	µA	V_{IN} = 0 to V_{CC}
Input low voltage	V_{IL}	—	—	0.2 V_{CC}	V	
Input high voltage	V_{IH}	0.5 V_{CC}	—	—	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.5 mA
Output high voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –400 µA
Forward threshold voltage ($\overline{EN}$, CLK)	V_{T+}	—	—	0.5 V_{CC}	V	
Backward threshold voltage ($\overline{EN}$, CLK)	V_{T-}	0.2 V_{CC}	—	—	V	

<Digital Part (V_{DD}) >

(V_{DD} = 2.7 to 5.5 V, Ta = –20 to +85°C, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	V_{DD}	2.7	3.0	5.5	V	
Input leak current	I_{ILK}	–10	—	10	µA	V_{IN} = 0 to V_{DD}
Input low voltage	V_{IL}	—	—	0.2 V_{DD}	V	
Input high voltage	V_{IH}	0.5 V_{DD}	—	—	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.5 mA
Output high voltage	V_{OH}	V_{DD} – 0.4	—	—	V	I_{OH} = –400 µA

Note: For circuit current of V_{DD}, see the analog block.

<Analog Part>

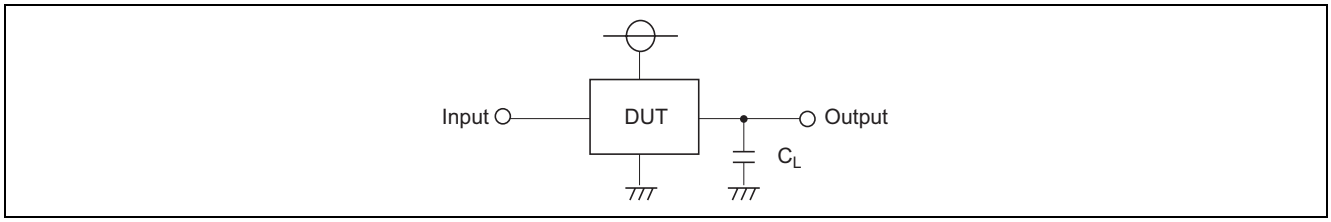
(V_{DD} (VrefU) = 2.7 to 5.5 V, Ta = –20 to +85°C, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Dissipation current	I_{DD}	—	1.5	3.5	mA	VrefU = 3 V input data condition: When maximum current of R-2R rudder is supplied
D/A converter upper reference voltage range	V_{DD} (VrefU)	2.7	—	5.5	V	In the setup range of reference voltage, all values are not taken with output. Values to be taken depend on the item of buffer amplifier output voltage range.
Buffer amplifier output voltage range	V_{AO}	0.1	—	V_{DD} – 0.1	V	I_{AO} = ±100 μA
		0.2	—	V_{DD} – 0.2	V	I_{AO} = +500 μA –200 μA
Buffer amplifier output drive range	I_{AO}	–0.3	—	1	mA	Upper saturation voltage = 0.4 V Lower saturation voltage = 0.4 V
Differential nonlinearity error	S_{DL}	–1.0	—	1.0	LSB	V_{DD} = 2.700 V (VrefU) Without load (I_{AO} = +0 μA)
Nonlinearity error	S_L	–1.5	—	1.5	LSB	
Zero code error	S_{ZERO}	–2	—	2	LSB	
Full scale error	S_{FULL}	–2	—	2	LSB	
Output capacitive load	C_O	—	—	10	μF	
Buffer amplifier output impedance	R_O	—	5	—	Ω	

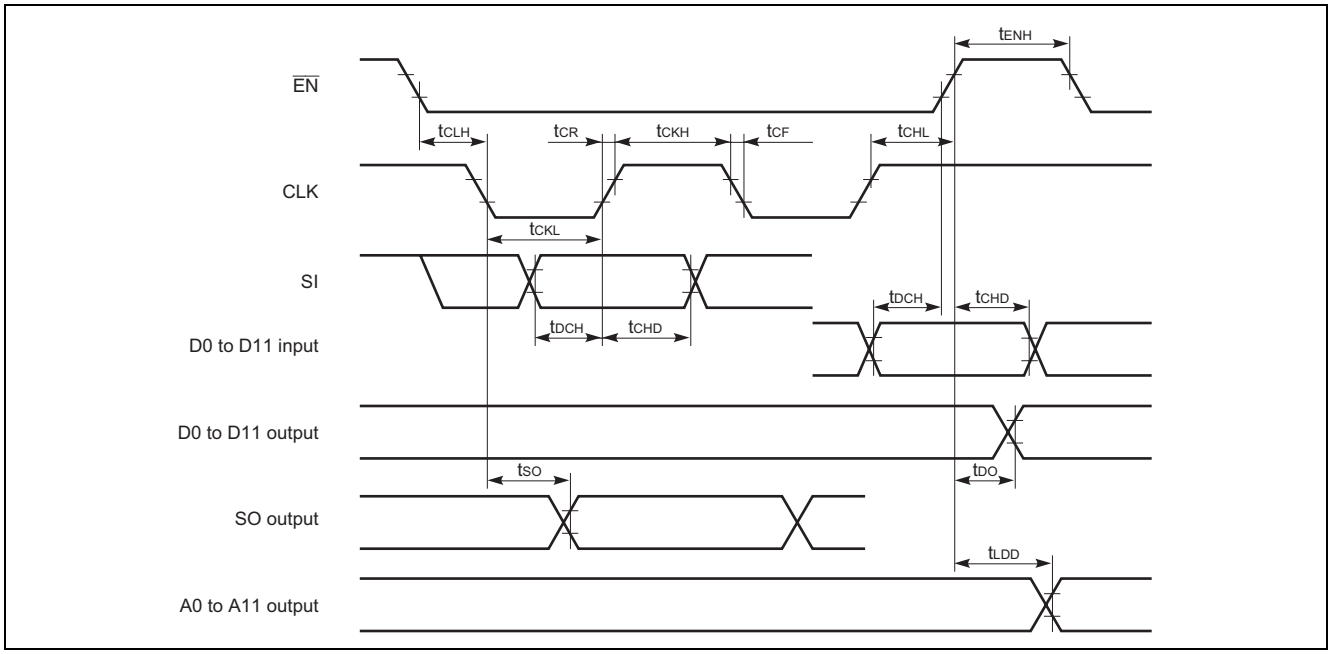
AC Characteristics

(V_{CC}, V_{DD} = 2.7 to 5.5 V, Ta = –20 to +85°C, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Clock low pulse width	t_{CKL}	200	—	—	ns	
Clock high pulse width	t_{CKH}	200	—	—	ns	
Clock rise time	t_{CR}	—	—	200	ns	
Clock fall time	t_{CF}	—	—	200	ns	
Data setup time	t_{DCH}	30	—	—	ns	
Data hold time	t_{CHD}	60	—	—	ns	
Clock ($\overline{EN}$) setup time	t_{CLH}	100	—	—	ns	
$\overline{EN}$ setup time	t_{CHL}	200	—	—	ns	
$\overline{EN}$ high hold time	t_{ENH}	200	—	—	ns	
Serial data output delay time	t_{SO}	—	200	350	ns	C_L = 100 pF
Parallel data output delay time	t_{DO}	—	400	600	ns	C_L = 100 pF
D/A output setting time	t_{LDD}	—	—	100	μs	$C_L \leq$ 100 pF, V_{AO}: 0.1 ↔ 2.6 V Until output takes ±2 LSB of the final value.

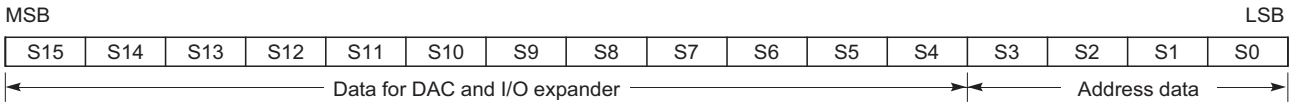


Timing Chart



Data Structure

Serial data



Address Data

S3	S2	S1	S0	Setup
0	0	0	0	(a)
0	0	0	1	A1 selection
0	0	1	0	A2 selection
0	0	1	1	A3 selection
0	1	0	0	A4 selection
0	1	0	1	A5 selection
0	1	1	0	A6 selection
0	1	1	1	A7 selection
1	0	0	0	A8 selection
1	0	0	1	A9 selection
1	0	1	0	A10 selection
1	0	1	1	A11 selection
1	1	0	0	A12 selection
1	1	0	1	I/O expander (serial → parallel conversion)
1	1	1	0	I/O expander (parallel → serial conversion)
1	1	1	1	I/O expander status setup

- I/O expander (serial → parallel conversion)
  Outputs data on S4 to S15 to pins D0 to D11.

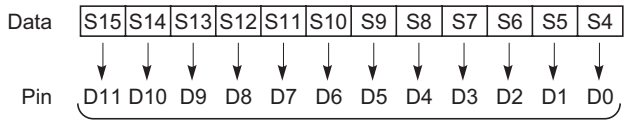
S3	S2	S1	S0
1	1	0	1

- I/O expander (parallel → serial conversion)
  Writes data on D0 to D11 pins into S4 to S15.
  When next data communication is provided, outputs data sequentially from SO pin at the rise of the shift clock (CLK).

S3	S2	S1	S0
1	1	1	0

- I/O expander status setup register
  Sets input/output pin of I/O expanders.
  Data: "0" = Input mode (Hi-Z status), "1" = Output mode

S3	S2	S1	S0
1	1	1	1



DAC Data

S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4*	Analog output voltage (Reference voltage on the lower side = 0.0 V fixed)	
0	0	0	0	0	0	0	0	X	X	X	0	$(V_{DD} / 256) \times 1$ [V]	(1 LSB)
0	0	0	0	0	0	0	1	X	X	X	0	$(V_{DD} / 256) \times 2$ [V]	(2 LSB)
0	0	0	0	0	0	1	0	X	X	X	0	$(V_{DD} / 256) \times 3$ [V]	(3 LSB)
:	:	:	:	:	:	:	:	:	:	:	:	:	
1	1	1	1	1	1	1	0	X	X	X	0	$(V_{DD} / 256) \times 255$ [V]	(255 LSB)
1	1	1	1	1	1	1	1	X	X	X	0	V_{DD} [V]	(256 LSB)
X	X	X	X	X	X	X	X	X	X	X	1	High-impedance (I/O expander selected)	

Note: X: Don't care
Only A5 to A12 outputs are available for DAC output by S4 and Hi-Z conversion.

(a) Command to set DAC output to High-impedance (DACHiZ command)

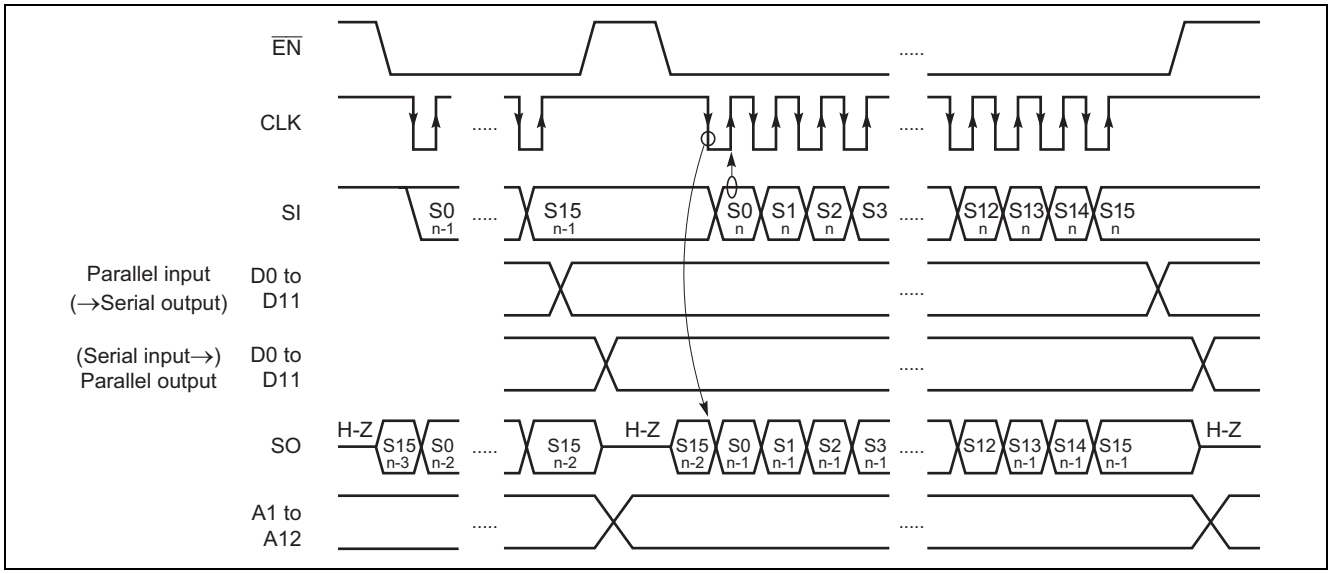
S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	Analog output voltage
X	X	X	X	X	X	X	X	1	1	0	1	0	0	0	0	Sets D/A output of A5 to A12 to High-impedance.

(b) Initial status just after power is turned on:
Low level output from A1 to A4 (set to 00h)
D4/A12 to D11/A5: DAC output of high-impedance (Hi-Z), I/O of input mode (Hi-Z)
D0 to D3: input mode (Hi-Z)

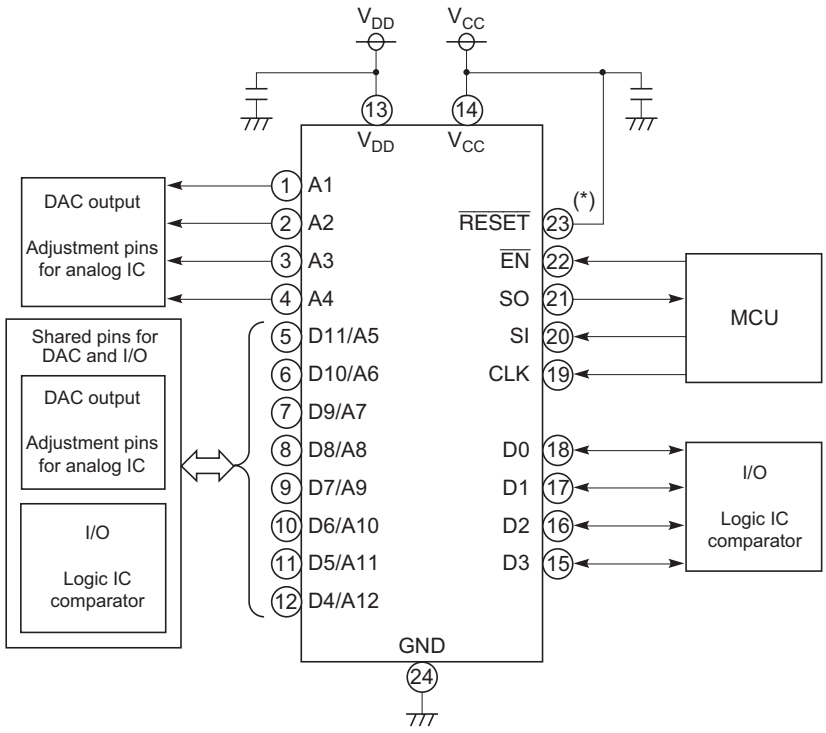
(c) The DACHiZ command is effective only for DAC settings (A5 to A12), but not for the I/O ports (D0 to D11)

Note: To change the status of pins D4/A12 to D11/A5, switch both analog and digital after setup of high-impedance.

Timing Chart (Model)



Application Example



Note: The $\overline{\text{RESET}}$ pin is directly connected with the power pin to use power-on reset. However, when forced reset is done from outside, the capacitance (0.1 to 10 μF) should be connected between $\overline{\text{RESET}}$ pin and ground to remove noise due to installation of line, etc.

Precaution for Use

This IC has two power supply pins and a ground pin. Superimposition of these pins with ripple and spike noise may cause reduction of conversion accuracy and occurrence of malfunction. Be sure to insert a capacitor between each power supply and the GND pin to stabilize D/A converting operation.

The output buffer amplifier of this IC has strong characteristics against capacitive load. Accordingly, when the capacitance (10 μF Max) is connected between output and ground to remove jitter and noise due to installation of output line, no problem may occur in operation of DAC. However, notice that the removal results in lengthening the settling time.

This IC also provides power-on reset function. To assure the resetting operation, power supply should be turned on in the order of timing shown in the diagram below.

Order: 1. $V_{CC} \rightarrow$ 2. V_{DD}

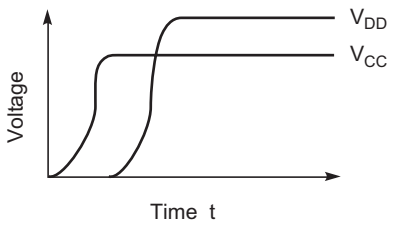
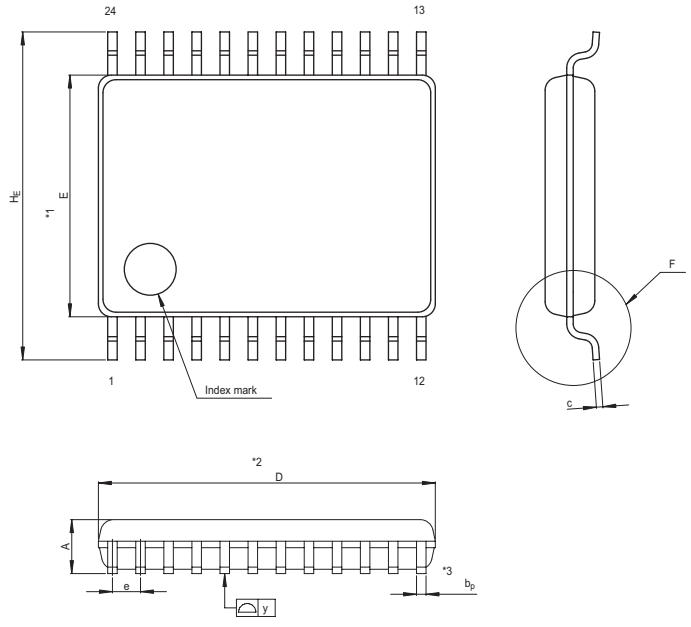


Figure 1 Order for Power-on

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP24-5.6x7.8-0.65	PLSP0024JA-A	24P2E-A	0.1g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	7.7	7.8	7.9
E	5.5	5.6	5.7
A_2	—	1.15	—
A	—	—	1.45
A_1	0	0.1	0.2
b_p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	7.4	7.6	7.8
e	0.53	0.65	0.77
y	—	—	0.10
L	0.3	0.5	0.7

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