

# Low-Dropout Linear Regulator Controller with PGOOD Indication

## General Description

The RT9194 is a low-dropout voltage regulator controller with a specific PGOOD indicating scheme, it acts as a power supervisor of the power regulated. The part could drive an external N-MOSFET for various applications accordingly; especially, the part is operated with V<sub>CC</sub> power ranging from 4.5V to 13.5V. With such a topology, it's with advantages of flexible and cost-effective. The part comes to a small footprint package of SOT-23-6.

## Ordering Information

RT9194 □□

- Package Type  
E : SOT-23-6
- Lead Plating System  
P : Pb Free  
G : Green (Halogen Free and Pb Free)

Note :

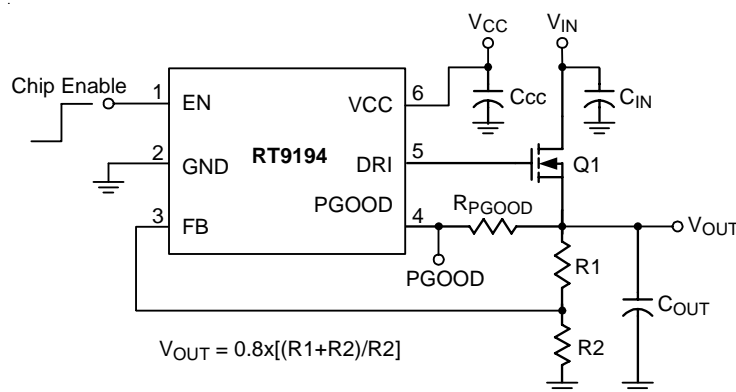
Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

## Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

## Typical Application Circuit



## Features

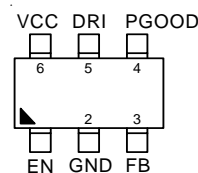
- 4.5V to 13.5V Operation Voltage
- High Accuracy ± 2% 0.8V Voltage Reference
- Quick Transient Response
- Power Good Indicator with Delay
- Enable Control
- Compliant with Intel "Grantsdale Chipset Platform Design Guide" Specification
- Small Footprint Package SOT-23-6
- RoHS Compliant and 100% Lead (Pb)-Free

## Applications

- Special Designed for Intel® Grantsdale platform FSB\_VTT power regulation
- Processor Power-Up Sequencing
- Notebook and laptop PC
- Other Power regulation with Power Good indication.

## Pin Configurations

(TOP VIEW)



SOT-23-6

Test Circuit

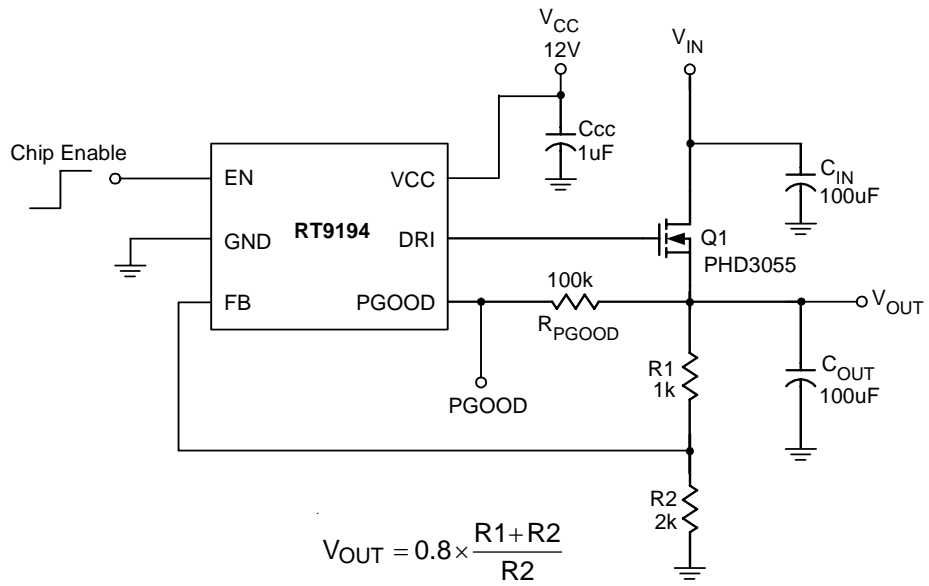


Figure 1. Typical Test Circuit

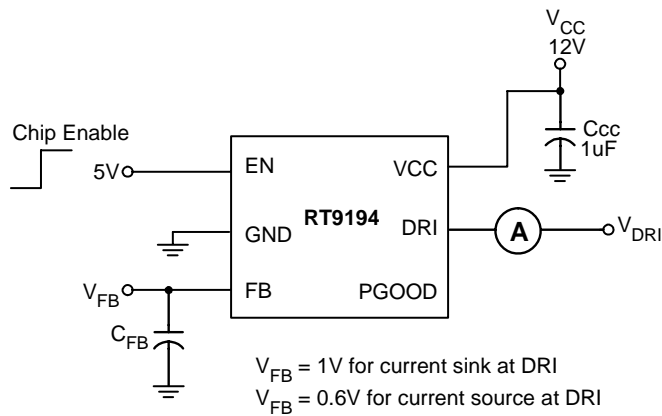
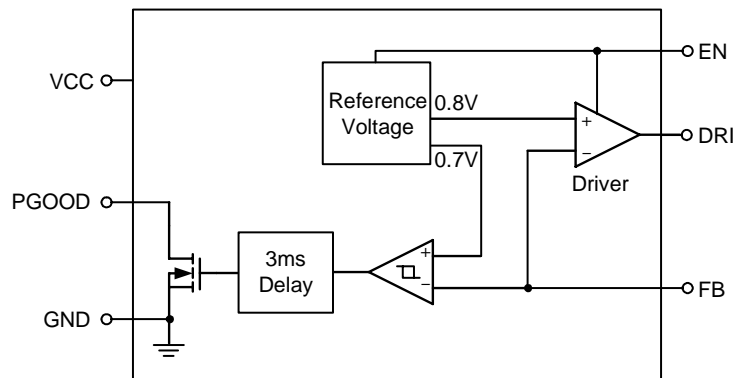


Figure 2. DRI Source/Sink Current Test Circuit

**Functional Pin Description**

Pin No.	Pin Name	Pin Function
1	EN	Chip Enable (Active High)
2	GND	Ground
3	FB	Output Voltage Feedback
4	PGOOD	Power Good Open Drain Output
5	DRI	Driver Output
6	VCC	Power Supply Input

**Function Block Diagram**



## Absolute Maximum Ratings (Note 1)

- Supply Input Voltage,  $V_{CC}$  ----- 15V
- Enable Voltage ----- 7V
- Power Good Output Voltage ----- 7V
- Power Dissipation,  $P_D$  @  $T_A = 25^\circ\text{C}$
- SOT-23-6 ----- 0.4W
- Package Thermal Resistance
- SOT-23-6,  $\theta_{JA}$  ----- 250°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 2)
- HBM (Human Body Mode) ----- 2kV
- MM (Machine Mode) ----- 200V

## Recommended Operating Conditions (Note 3)

- Supply Input Voltage,  $V_{CC}$  ----- 4.5V to 13.5V
- Enable Voltage ----- 0V to 5.5V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

## Electrical Characteristics

( $V_{CC} = 5V/12V$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
$V_{CC}$ Operation Voltage Range		$V_{CC}$ input range	4.5	--	13.5	V
POR Threshold		$V_{CC}$ rising	4.0	4.2	4.5	V
POR Hysteresis		$V_{CC}$ falling	--	0.2	--	V
$V_{CC}$ Supply Current		$V_{CC} = 12V$	--	0.3	0.8	mA
Driver Source Current		$V_{CC} = 12V$ , $V_{DRI} = 6V$	5	--	--	mA
Driver Sink Current		$V_{CC} = 12V$ , $V_{DRI} = 6V$	5	--	--	mA
Reference Voltage ( $V_{FB}$ )		$V_{CC} = 12V$ , $V_{DRI} = 5V$	0.784	0.8	0.816	V
Reference Line Regulation ( $V_{FB}$ )		$V_{CC} = 4.5V$ to $15V$	--	3	6	mV
Amplifier Voltage Gain		$V_{CC} = 12V$ , no load	--	70	--	dB
PSRR at 100Hz, No Load		$V_{CC} = 12V$ , no load	50	--	--	dB
<b>Power Good</b>						
Rising Threshold		$V_{CC} = 12V$	--	90	--	%
Hysteresis		$V_{CC} = 12V$	--	15	--	%
Sink Capability		$V_{CC} = 12V$ @ 1mA	--	0.2	0.4	V
Delay Time		$V_{CC} = 12V$	1	3	10	ms
Falling Delay		$V_{CC} = 12V$	--	15	--	us

*To be Continued*

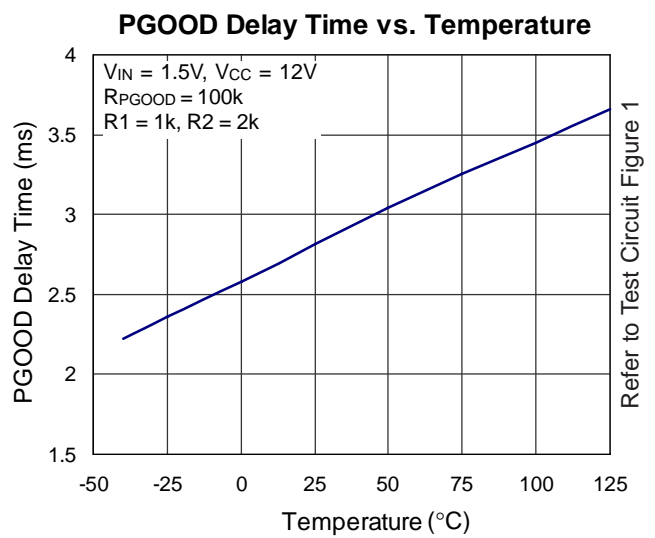
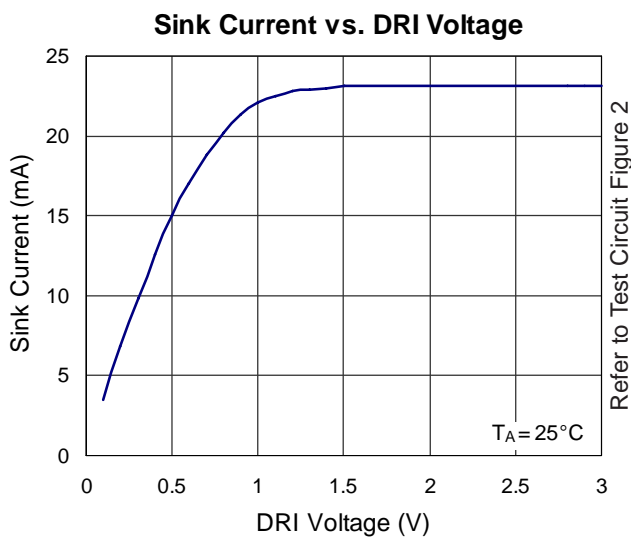
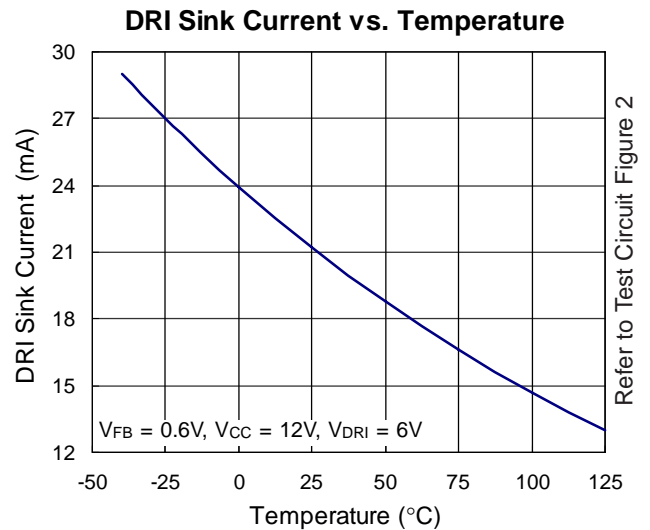
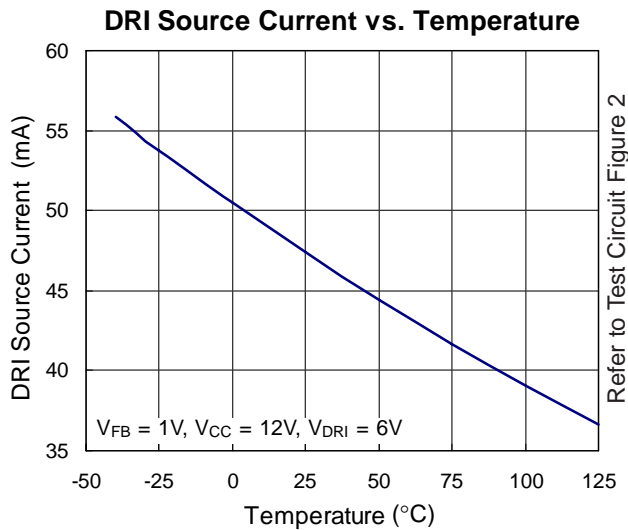
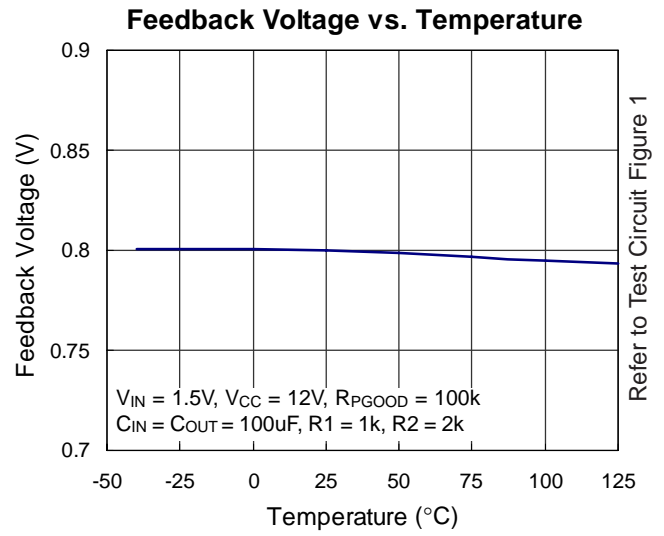
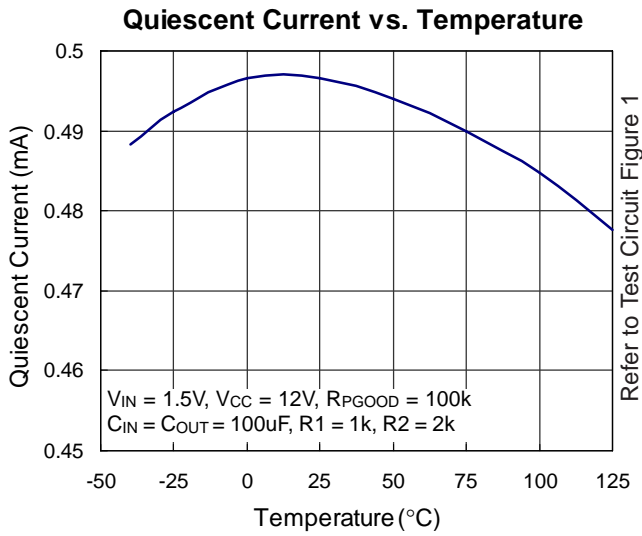
Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Chip Enable</b>					
EN Rising Threshold	$V_{CC} = 12V$	--	0.7	--	V
EN Hysteresis	$V_{CC} = 12V$	--	30	--	mV
Standby Current	$V_{CC} = 12V, V_{EN} = 0V$	--	--	5	$\mu A$

**Note 1.** Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

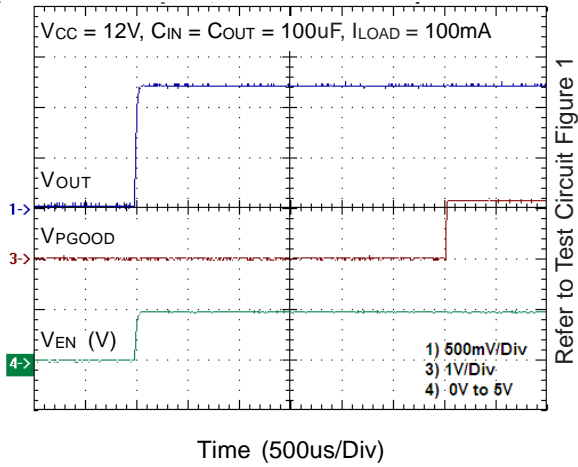
**Note 2.** Devices are ESD sensitive. Handling precaution recommended.

**Note 3.** The device is not guaranteed to function outside its operating conditions.

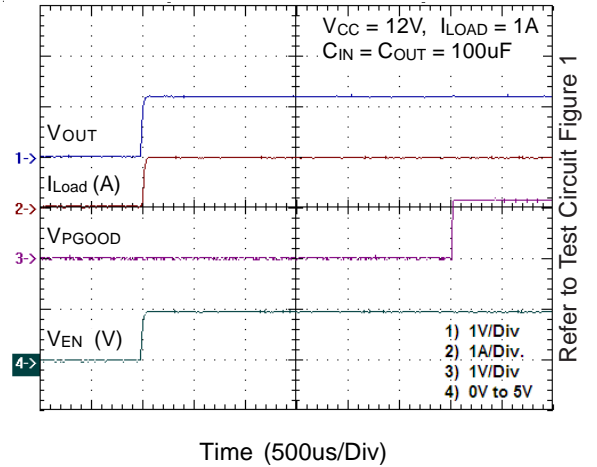
Typical Operating Characteristics



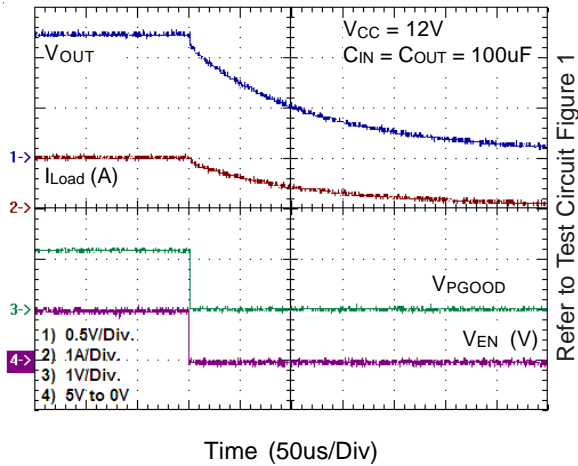
**PGOOD Delay Time**



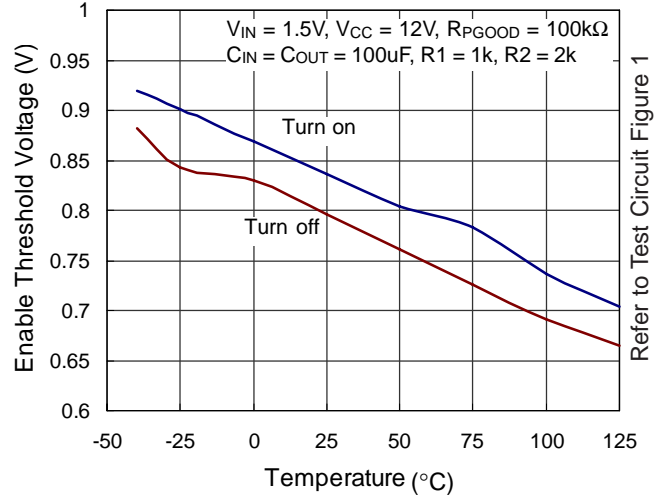
**PGOOD Delay Time**



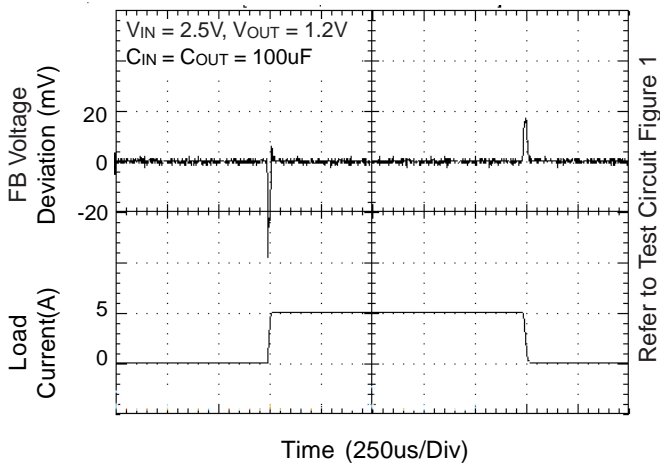
**PGOOD Off**



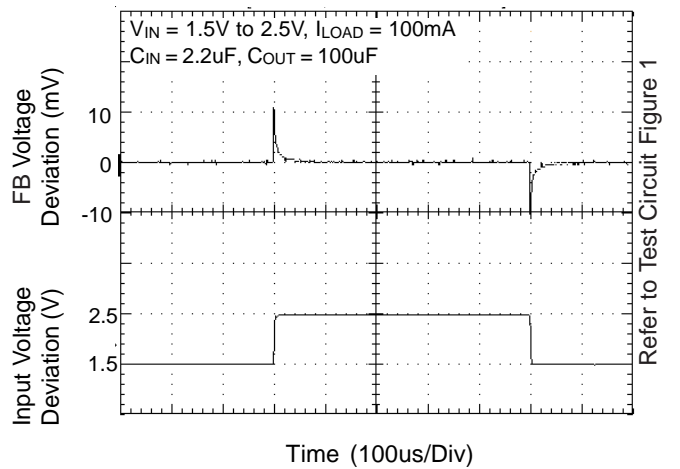
**Enable Threshold Voltage vs. Temperature**



**Load Transient Response**



**Line Transient Response**



## Application Information

### Capacitors Selection

Careful selection of the external capacitors for RT9194 is highly recommended in order to remain high stability and performance.

Regarding the supply voltage capacitor, connecting a capacitor which is 1 $\mu$ F between V<sub>CC</sub> and ground is a must. The capacitor improves the supply voltage stability to provide chip normally operating.

Regarding the input capacitor, connecting a capacitor which 100 $\mu$ F between V<sub>IN</sub> and ground is recommended to increase stability. With large value of capacitance could result in better performance for both PSRR and line transient response.

When driving external pass element, connecting a capacitor 100 $\mu$ F between V<sub>OUT</sub> and ground is recommended for stability. With larger capacitance can reduce noise and improve load transient response and PSRR.

### Output Voltage Setting

The RT9194 develop a 0.8V reference voltage; especially suit for low voltage application. As shown in application circuit, the output voltage could easy set the output voltage by R1 & R2 divider resistor.

### Power Good Function

The RT9194 has the power good function with delay. The power good output is an open drain output. Connect a 100k $\Omega$  pull up resistor to V<sub>OUT</sub> to obtain an output voltage. When the output voltage arrive 90% of normal value the power good will output voltage with 3ms delay time.

When the output voltage falling arrive 75% of normal value the power good will turn off with less than 1ms delay time. But, there are two exceptions. One is the enable pull low the power good will turn off quickly. The second is the V<sub>CC</sub> falling arrive POR value (4V typ.) the power good also will turn off quickly.

### Chip Enable Operation

Pull the EN pin low to drive the device into shutdown mode. During shutdown mode, the standby current drops to 5 $\mu$ A<sub>(MAX)</sub>. The external capacitor and load current determine

the output voltage decay rate. Drive the EN pin high to turn on the device again.

### Under Voltage Protection

RT9194 equips the V<sub>OUT</sub> under-voltage (UV) protection function. The UV protection circuits will start monitoring the power status after the PGOOD pin goes high. If the output voltage drops to below 75% of its setting value, the PGOOD and DRI pins will be pulled low and latch RT9194. The UV latch status will be released only when V<sub>CC</sub> or Enable pin goes low and returns high again, which will also cause RT9194 to re-activate.

### MOSFET Selection

The RT9194 are designed to driver external N-Channel MOSFET pass element. MOSFET selection criteria include threshold voltage V<sub>GS</sub> (V<sub>TH</sub>), maximum continuous drain current I<sub>D</sub>, on-resistance R<sub>DS(ON)</sub>, maximum drain-to-source voltage V<sub>DS</sub> and package thermal resistance  $\theta_{(JA)}$ .

The most critical specification is the MOSFET R<sub>DS(ON)</sub>. Calculate the required R<sub>DS(ON)</sub> from the following formula:

$$\text{NMOSFET } R_{DS(ON)} = \frac{V_{IN} - V_{OUT}}{I_{LOAD}}$$

For example, the MOSFET operate up to 2A when the input voltage is 1.5V and set the output voltage is 1.2V, R<sub>ON</sub> = (1.5V-1.2V) / 2A = 150m $\Omega$ , the MOSFET's R<sub>ON</sub> have to select lower than 150m $\Omega$ . A Philip PHD3055E MOSFET with an R<sub>DS(ON)</sub> of 120m $\Omega$ (typ.) is a close match.

And carry on consider the thermal resistance from junction to ambient  $\theta_{(JA)}$  of the MOSFET's package. The power dissipation calculate by :

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD}$$

The thermal resistance from junction to ambient  $\theta_{(JA)}$  calculate by :

$$\theta_{(JA)} = \frac{(T_J - T_A)}{P_D}$$

In this example, P<sub>D</sub> = (1.5V - 1.2V) x 2A = 0.6W. The PHD3055E's  $\theta_{(JA)}$  is 75 $^{\circ}$ C/W for its D-PAK package, which translates to a 45 $^{\circ}$ C temperature rise above ambient. The package provides exposed backsides that directly transfer heat to the PCB board.



**PNP Transistor Selection**

The RT9194 could driver the PNP transistor to sink output current. PNP transistor selection criteria include DC current gain  $h_{FE}$ , threshold voltage  $V_{EB}$ , collector-emitter voltage  $V_{CE}$ , maximum continues collector current  $I_C$ , package thermal resistance  $\theta_{(JA)}$ .

For example, the PNP transistor operates sink current up to 0.5A when the input voltage is 1.5V and set the output voltage is 1.2V. As show in Figure 3. A KSB772 PNP transistor, the  $V_{CE} = 1.2V$ ,  $V_{BE} = -1V$ ,  $I_C = 0.5A$ ,  $I_B = 0.5/160 \geq 3.125mA$ , when the DRI pin voltage is 0.2V could sink  $6.8mA_{(MAX)}$  is a close match.

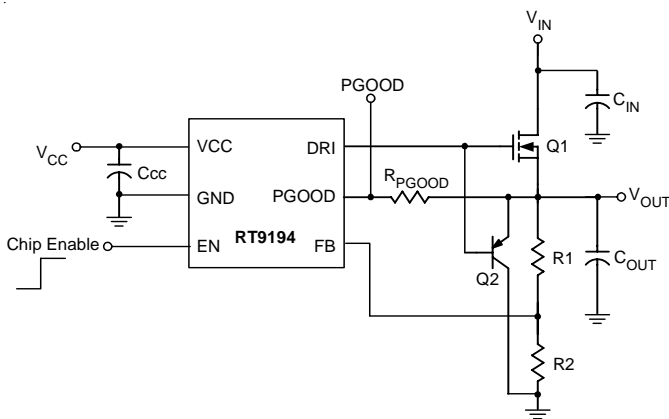


Figure 3

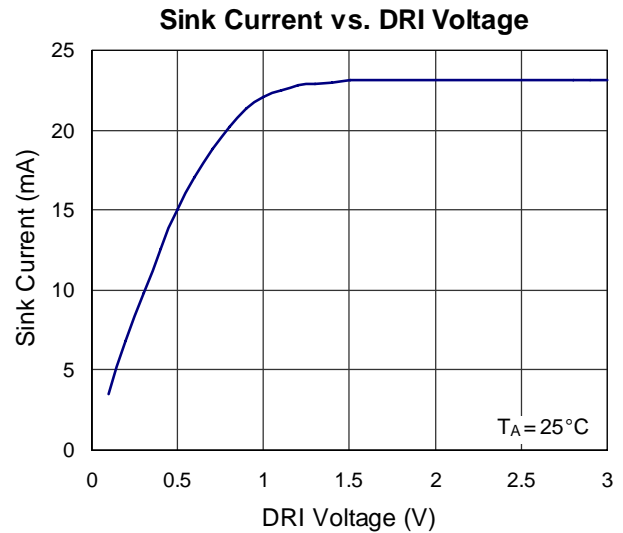


Figure 4

**Layout Considerations**

There are three critical layout considerations. One is the divider resistors should be located to RT9194 as possible to avoid inducing any noise. The second is capacitors place. The  $C_{IN}$  and  $C_{OUT}$  have to put at near the NMOS for improve performance. The third is the copper area for pass element. We have to consider when the pass element operating under high power situation that could rise the junction temperature. In addition to the package thermal resistance limit, we could add the copper area to improve the power dissipation. As show in Figure 5 and Figure 6.

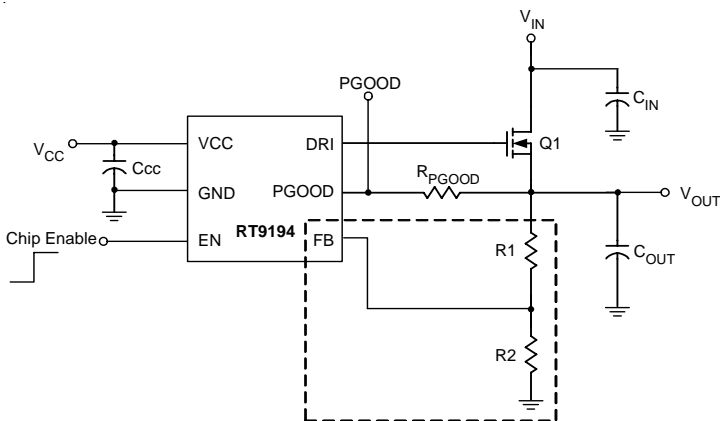


Figure 5

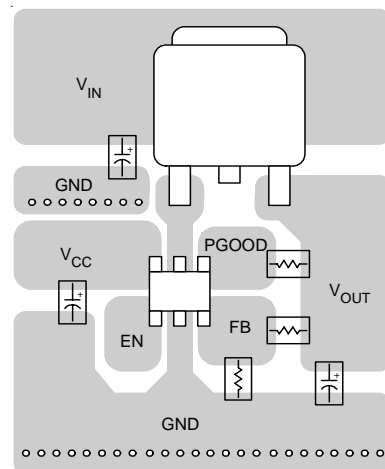
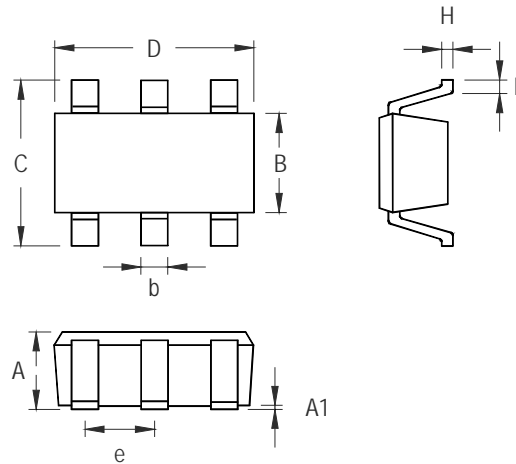


Figure 6

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

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