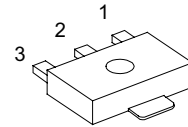


**Sensitive Gate
Silicon Controlled Rectifiers
Reverse Blocking Thyristors**

PNPN devices designed for high volume, line-powered consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic SOT-89 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Allows Triggering by Microcontrollers and Other Logic Circuits
- Blocking Voltage to 800 V
- On-State Current Rating of 0.8 Amperes RMS at 80°C
- High Surge Current Capability — 10 A
- Minimum and Maximum Values of IGT, VGT and IH Specified for Ease of Design
- Immunity to dV/dt — 20 V/μsec Minimum at 110°C
- Glass-Passivated Surface for Reliability and Uniformity

SCR
0.8 AMPERES RMS
300 thru 800 VOLTS



SOT-89

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage ^(Note 1) ($T_J = -40$ to 110°C , Sine Wave, 50 to 60 Hz; Gate Open) CR05AS-3 CR05AS-4 CR05AS-6 CR05AS-8	V_{DRM} , V_{RRM}	300 400 600 800	V
On-State RMS Current ($T_C = 80^\circ\text{C}$) 180° Conduction Angles	$I_{T(RMS)}$	0.8	A
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, $T_J = 25^\circ\text{C}$)	I_{TSM}	10	A
Circuit Fusing Consideration ($t = 8.3$ ms)	I^2t	0.415	A ² s
Forward Peak Gate Power ($T_A = 25^\circ\text{C}$, Pulse Width ≤ 1.0 μs)	P_{GM}	0.1	W
Forward Average Gate Power ($T_A = 25^\circ\text{C}$, $t = 8.3$ ms)	$P_{G(AV)}$	0.10	W
Forward Peak Gate Current ($T_A = 25^\circ\text{C}$, Pulse Width ≤ 1.0 μs)	I_{GM}	1.0	A
Reverse Peak Gate Voltage ($T_A = 25^\circ\text{C}$, Pulse Width ≤ 1.0 μs)	V_{GRM}	5.0	V
Operating Junction Temperature Range @ Rate V_{RRM} and V_{DRM}	T_J	-40 to 110	°C
Storage Temperature Range	T_{stg}	-40 to 150	°C

PIN ASSIGNMENT	
1	Gate
2	Anode
3	Cathode

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant source such that the voltage ratings of the devices are exceeded.

CR05AS Series

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction-to-Case – Junction-to-Ambient	$R_{\theta JC}$ $R_{\theta JA}$	75 200	$^{\circ}C/W$
Lead Solder Temperature ($< 1/16''$ from case, 10 secs max)	T_L	260	$^{\circ}C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Peak Repetitive Forward or Reverse Blocking Current ^(Note 2) $T_C = 25^{\circ}C$ ($V_D = \text{Rated } V_{DRM}$ and V_{RRM} ; $R_{GK} = 1 \text{ k}\Omega$) $T_C = 110^{\circ}C$	I_{DRM}, I_{RRM}	— —	— —	10 100	μA
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ON CHARACTERISTICS

Peak Forward On-State Voltage* ($I_{TM} = 1.0 \text{ A Peak @ } T_A = 25^{\circ}C$)	V_{TM}	—	—	1.7	V
Gate Trigger Current (Continuous dc) ^(Note 3) ($V_{AK} = 7.0 \text{ Vdc}, R_L = 100 \Omega$)	I_{GT}	—	40	200	μA
Holding Current ⁽²⁾ ($V_{AK} = 7.0 \text{ Vdc}, \text{Initiating Current} = 20 \text{ mA}$)	I_H	— —	0.5 —	5.0 10	mA
Latch Current ($V_{AK} = 7.0 \text{ V}, I_g = 200 \mu A$)	I_L	— —	0.6 —	10 15	mA
Gate Trigger Voltage (Continuous dc) ^(Note 3) ($V_{AK} = 7.0 \text{ Vdc}, R_L = 100 \Omega$) $T_C = -40^{\circ}C$	V_{GT}	— —	0.62 —	0.8 1.2	V

DYNAMIC CHARACTERISTICS

Critical Rate of Rise of Off-State Voltage ($V_D = \text{Rated } V_{DRM}$, Exponential Waveform, $R_{GK} = 1000 \Omega, T_J = 110^{\circ}C$)	dV/dt	20	35	—	$V/\mu s$
Critical Rate of Rise of On-State Current ($I_{PK} = 20 \text{ A}; P_w = 10 \mu s; di/dt = 1 \text{ A}/\mu s; I_{gt} = 20 \text{ mA}$)	di/dt	—	—	50	$A/\mu s$

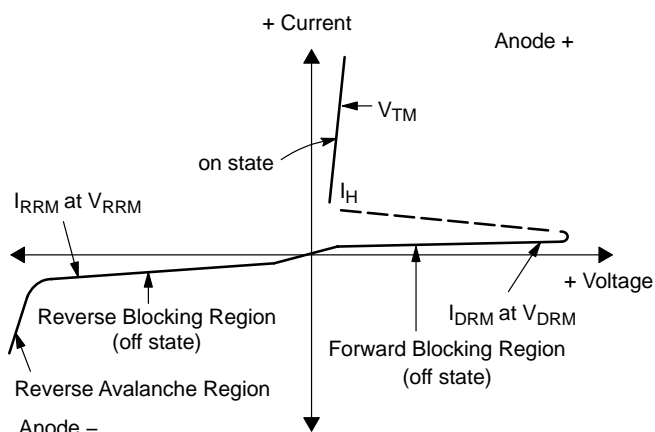
*Indicates Pulse Test: Pulse Width $\leq 1.0 \text{ ms}$, Duty Cycle $\leq 1\%$.

2. $R_{GK} = 1000 \Omega$ included in measurement.

3. Does not include R_{GK} in measurement.

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak on State Voltage
I_H	Holding Current



CR05AS Series

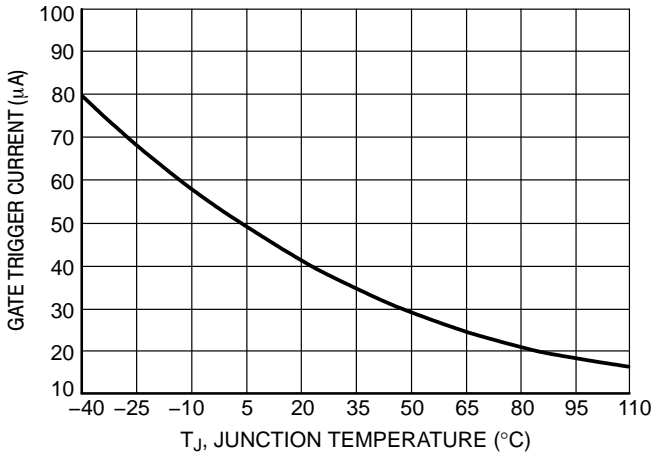


Figure 1. Typical Gate Trigger Current versus Junction Temperature

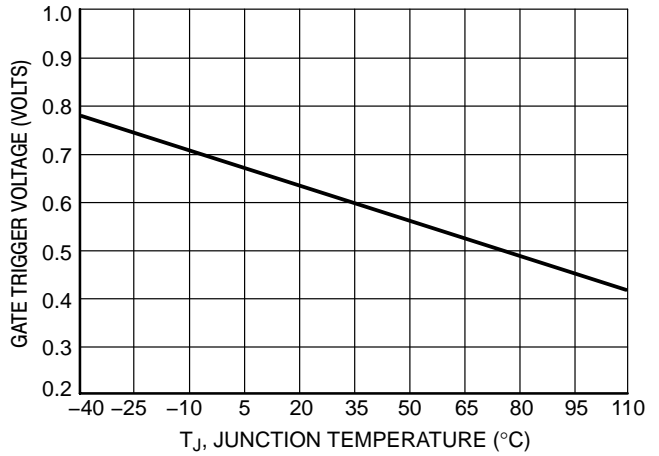


Figure 2. Typical Gate Trigger Voltage versus Junction Temperature

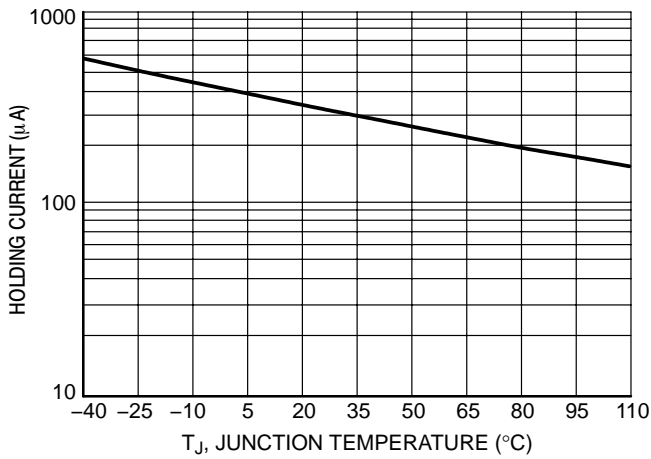


Figure 3. Typical Holding Current versus Junction Temperature

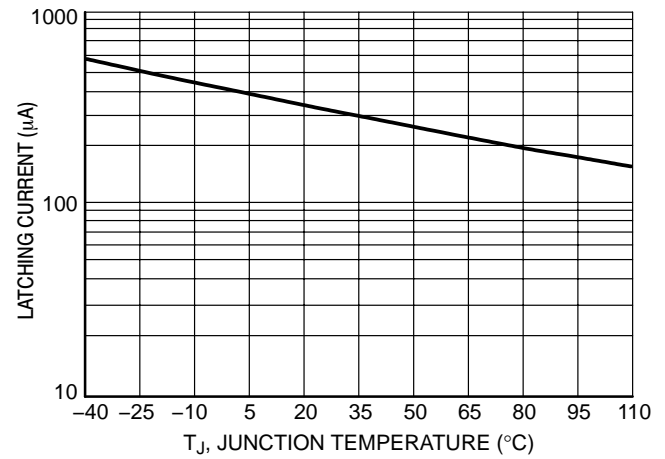


Figure 4. Typical Latching Current versus Junction Temperature

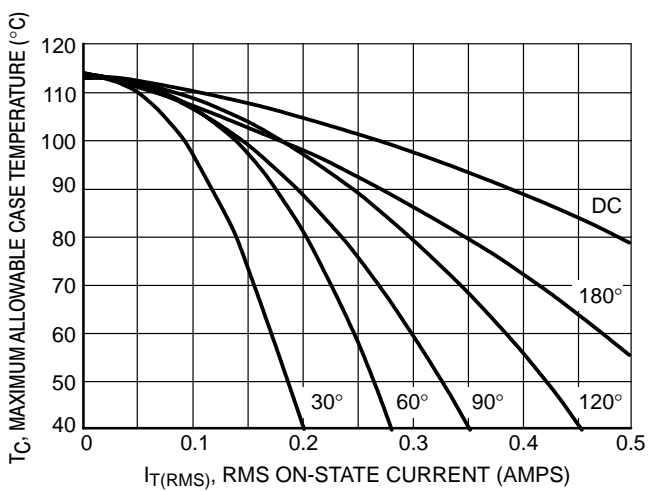


Figure 5. Typical RMS Current Derating

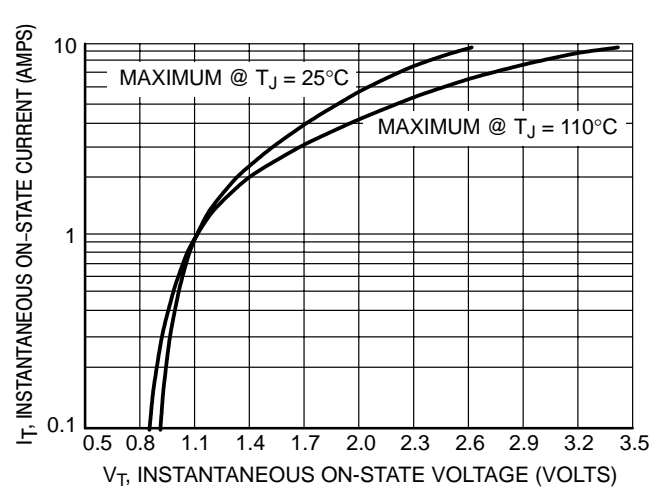


Figure 6. Typical On-State Characteristics